

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Akihiro NITAYAMA et al.

Serial No: 09/660,390

Filed: September 12, 2000

For: DYNAMIC SEMICONDUCTOR MEMORY DEVICE HAVING  
A TRENCH CAPACITOR AND METHOD OF MANUFACTURING  
THE SAME

Group Art No. 2814

Examiner: H. Weiss

Docket No. 000629.00002

#11/E/D  
7/16/02  
Linder

SUBMISSION OF CORRECTED FORMAL DRAWINGS

Assistant Commissioner for Patents  
Washington, D.C. 20231

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JUL -3 2002  
TECHNOLOGY CENTER 2800

Sir:

In accordance with the final Office Action dated May 1, 2002, submitted herewith are fifty-four (54) sheets of formal corrected drawings (Figs. 1a-33). These drawings include the changes to Figs. 1a, 1b, 2a and 2b, as set forth in the proposed drawing correction filed March 18, 2002, which were approved in the final Action.

Respectfully submitted,

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for Joseph M. Potenza  
Registration No. 28,175

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1001 G Street, N.W., 11<sup>th</sup> Floor  
Washington, D.C. 20001  
(202) 508-9100

Date: July 1, 2002

Figure 1A

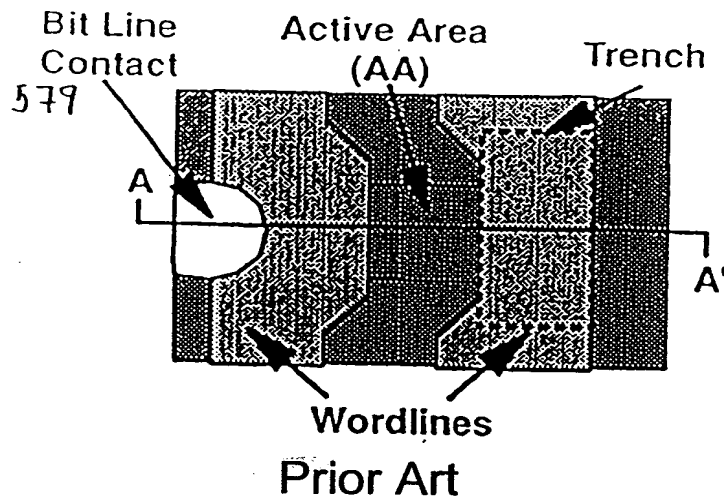
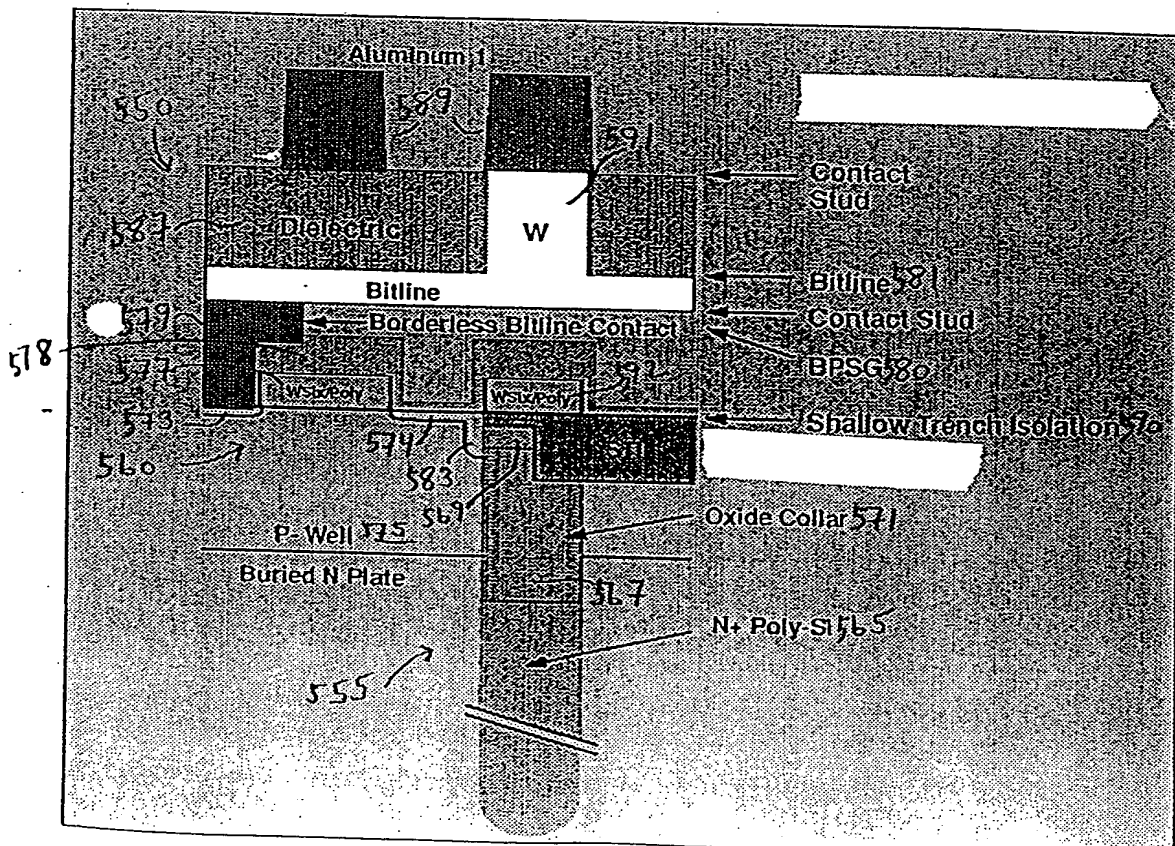


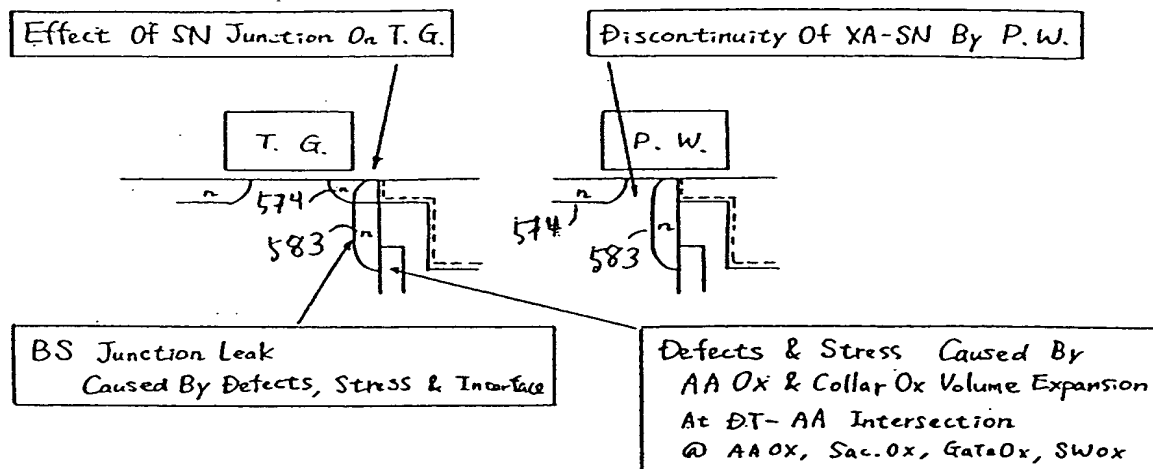
Figure 1B



Prior Art

Figure 2A

Figure 2B



Prior Art

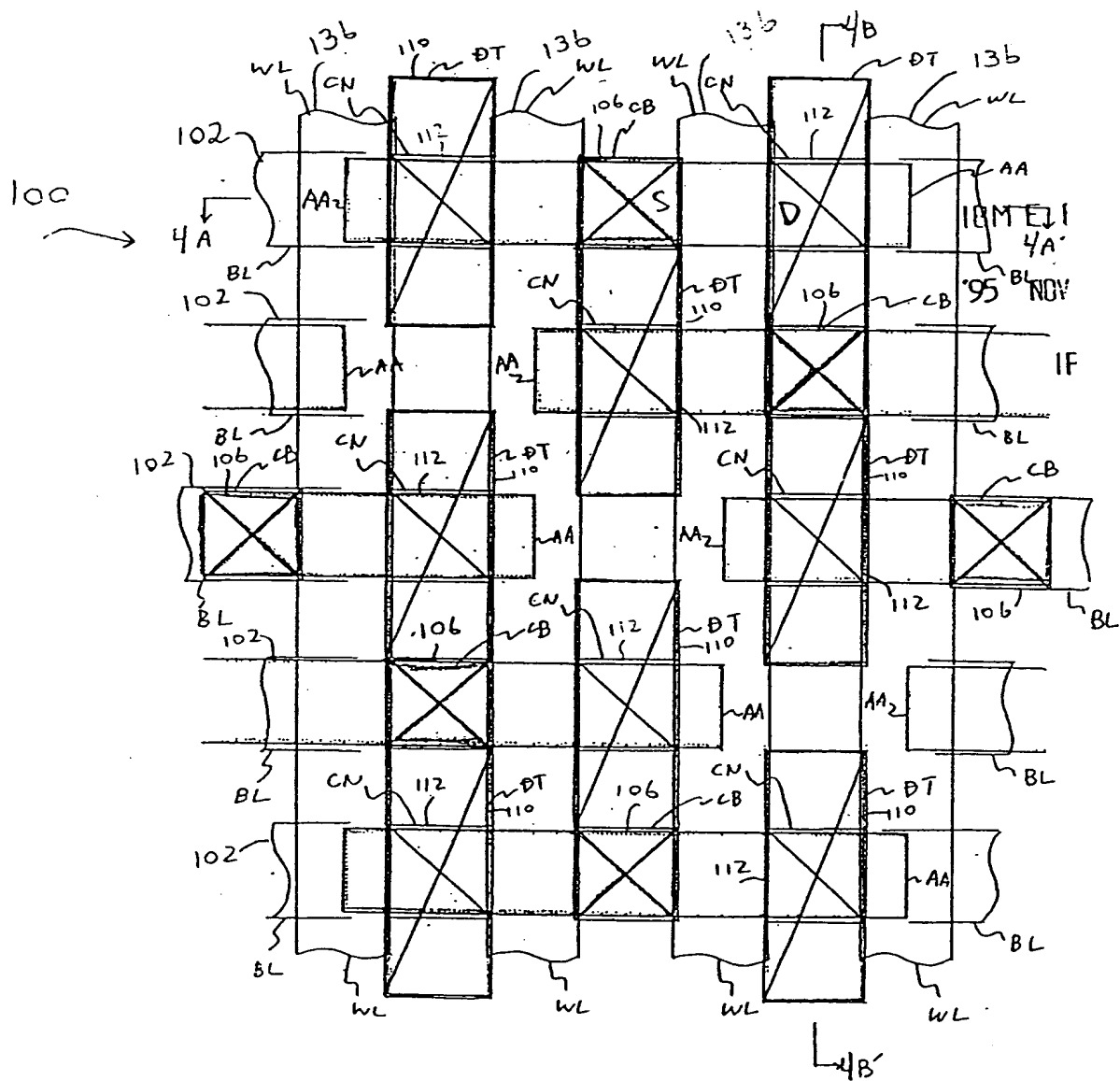
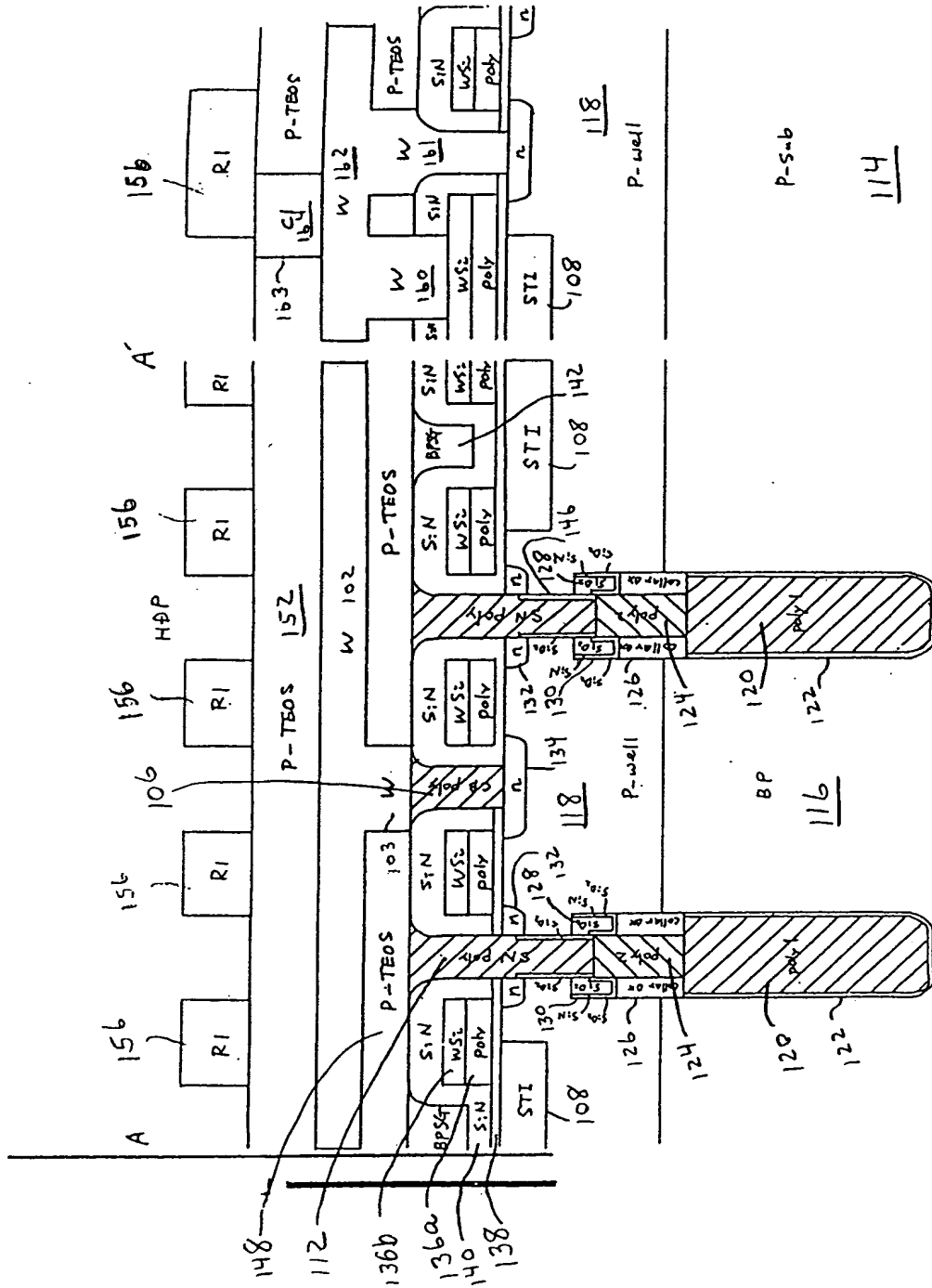


Figure 3

Figure 4A



— Cell Array —

— Support Circuit —

Figure 4B

HDP

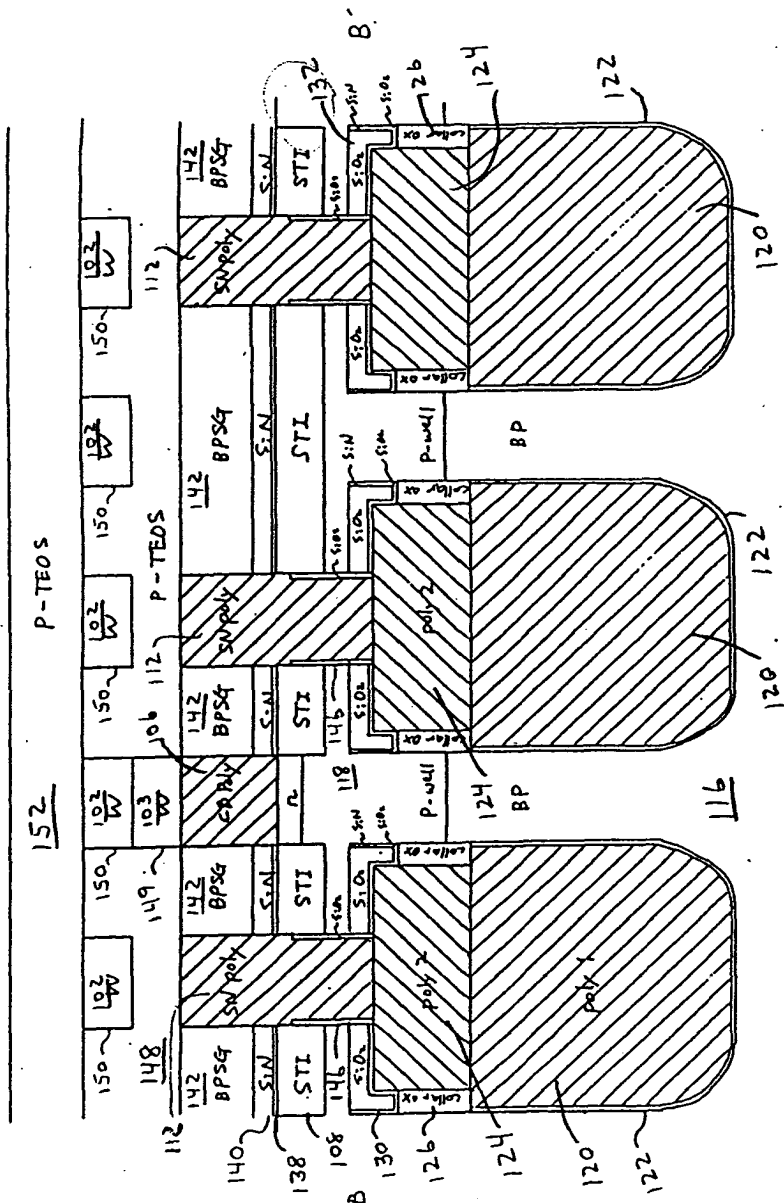


Figure 5A

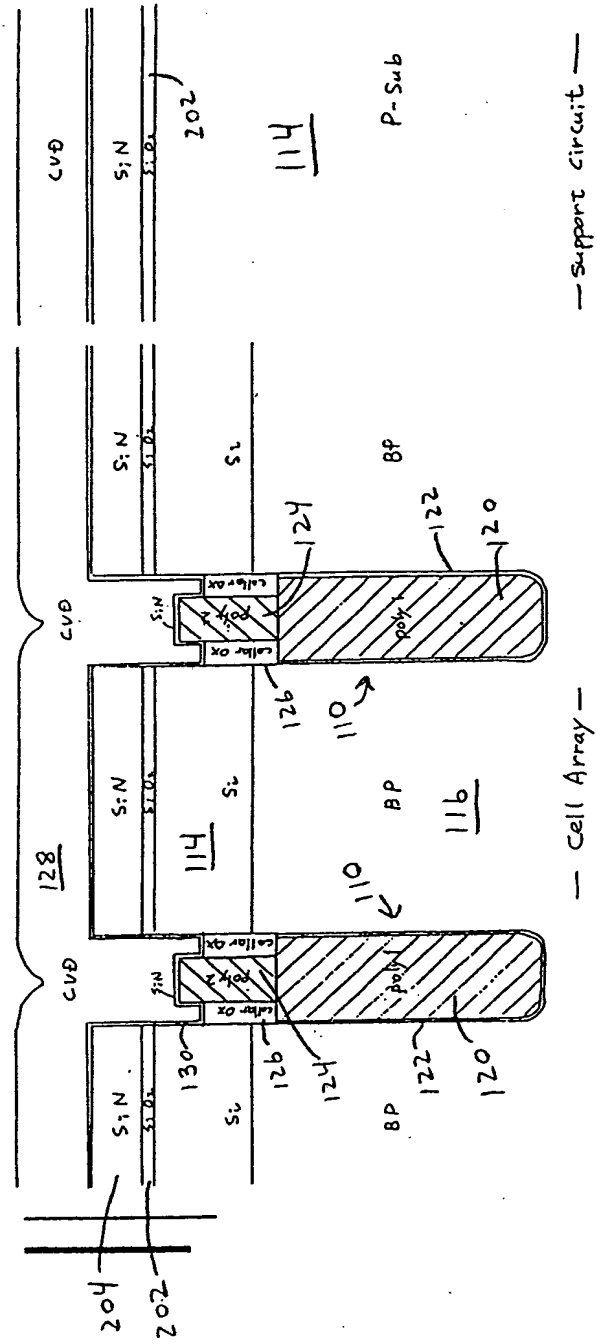


Figure 5B

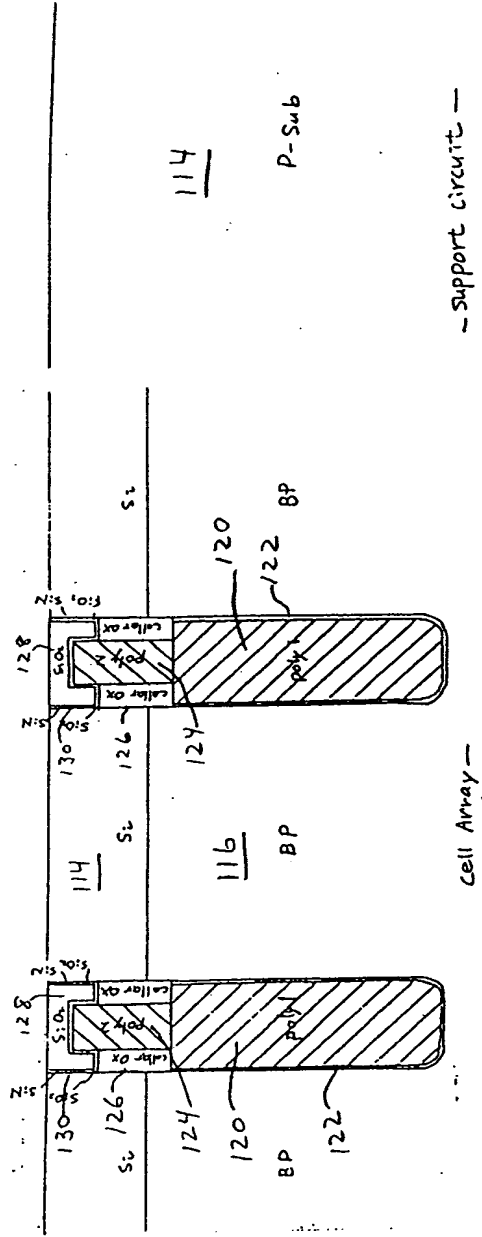


Figure 5C

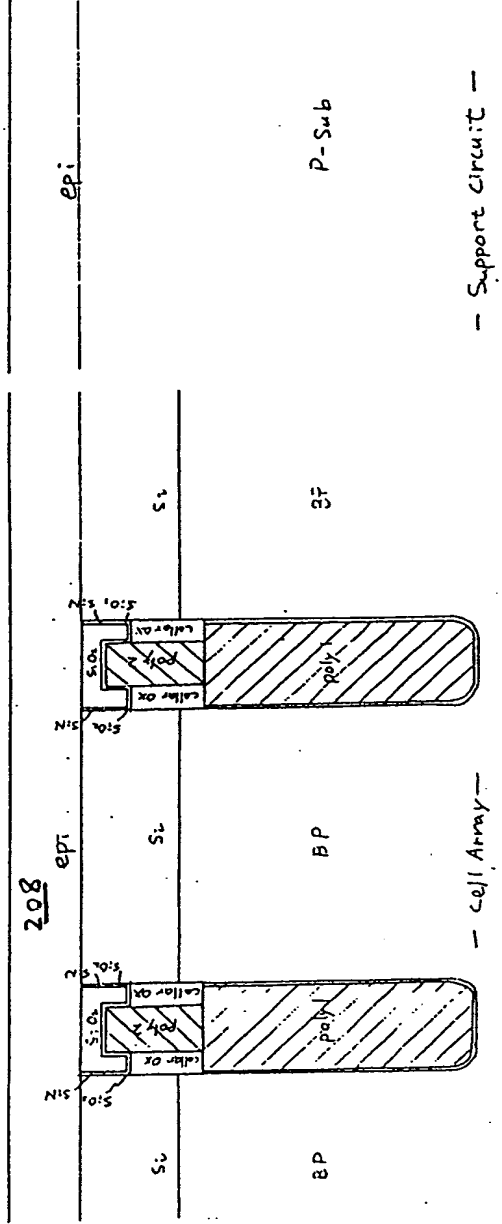
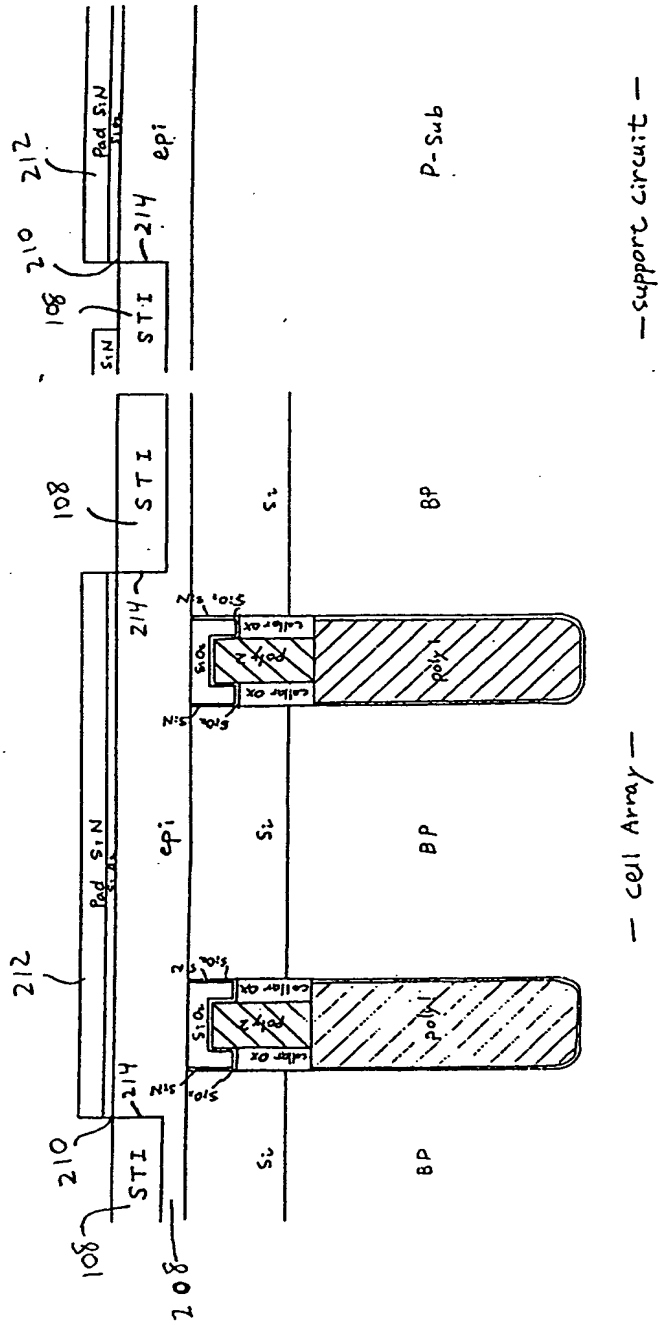




Figure 5D



The diagram illustrates a semiconductor device structure, likely a MOSFET, with various layers and regions labeled. The structure is shown in cross-section and a top-down view.

**Top-down view (left):** Shows a central region labeled **118** (P-well) surrounded by a **P-Sub** (P-Substrate). The structure includes a **STI** (Shallow Trench Isolation) region, a **poly** (polysilicon) gate, and a **BSG** (Buried Silicon Gate) region. The layers are labeled **SiN** (Silicon Nitride), **WSi** (Wet Silicon), and **poly** (polysilicon). The regions are numbered **136**, **142**, **132**, and **134**.

**Cross-section (right):** Shows a cross-section of the device. The central region is labeled **118** (P-well) and is surrounded by a **P-Sub** (P-Substrate). The structure includes a **STI** (Shallow Trench Isolation) region, a **poly** (polysilicon) gate, and a **BSG** (Buried Silicon Gate) region. The layers are labeled **SiN** (Silicon Nitride), **WSi** (Wet Silicon), and **poly** (polysilicon). The regions are numbered **136**, **142**, **132**, and **134**.

**Labels:** **118**, **P-well**, **P-Sub**, **STI**, **poly**, **BSG**, **SiN**, **WSi**, **136**, **142**, **132**, **134**.

— Support Circuit —.

P-Sub

P-well



Figure 5g

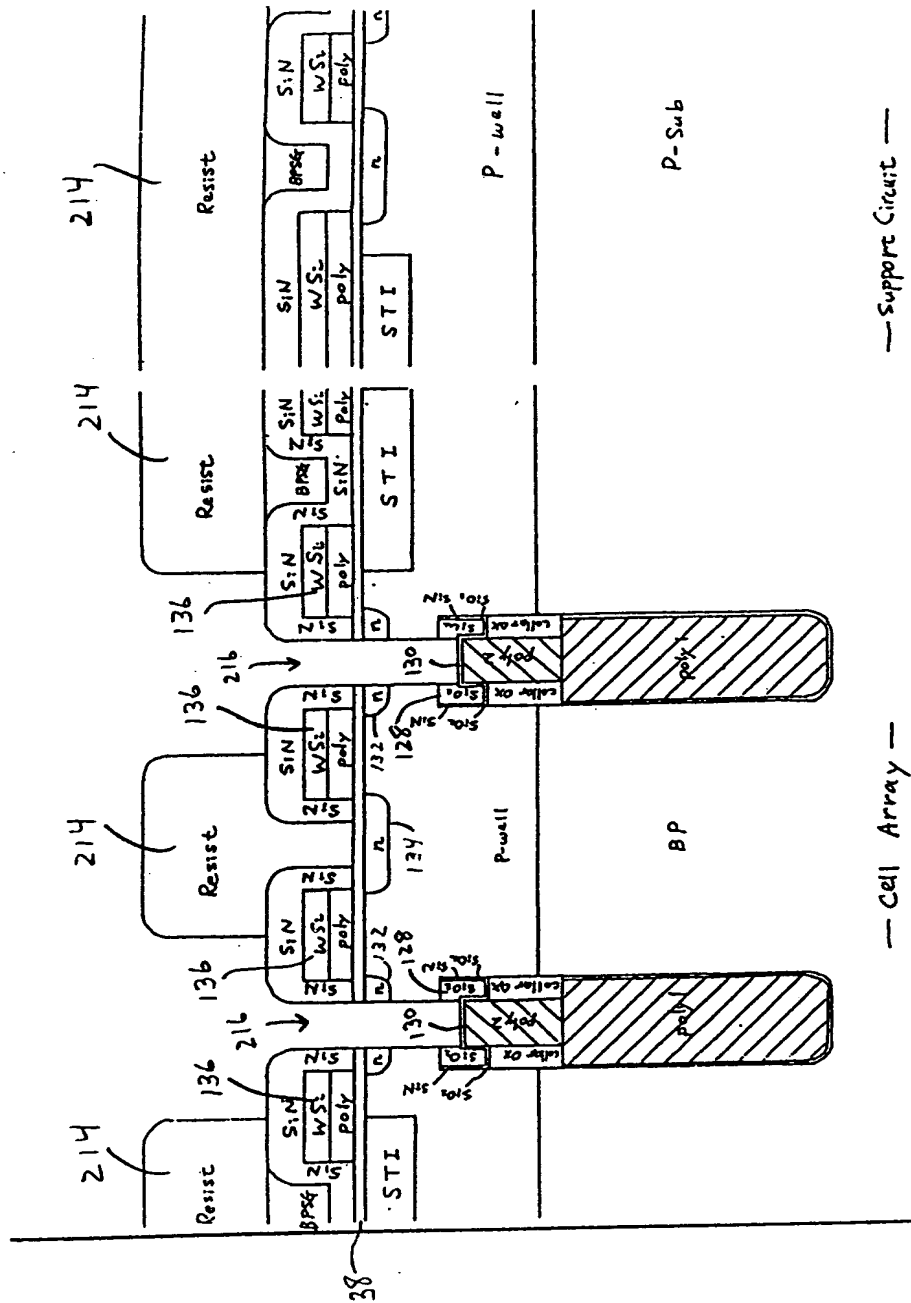


Figure 5H

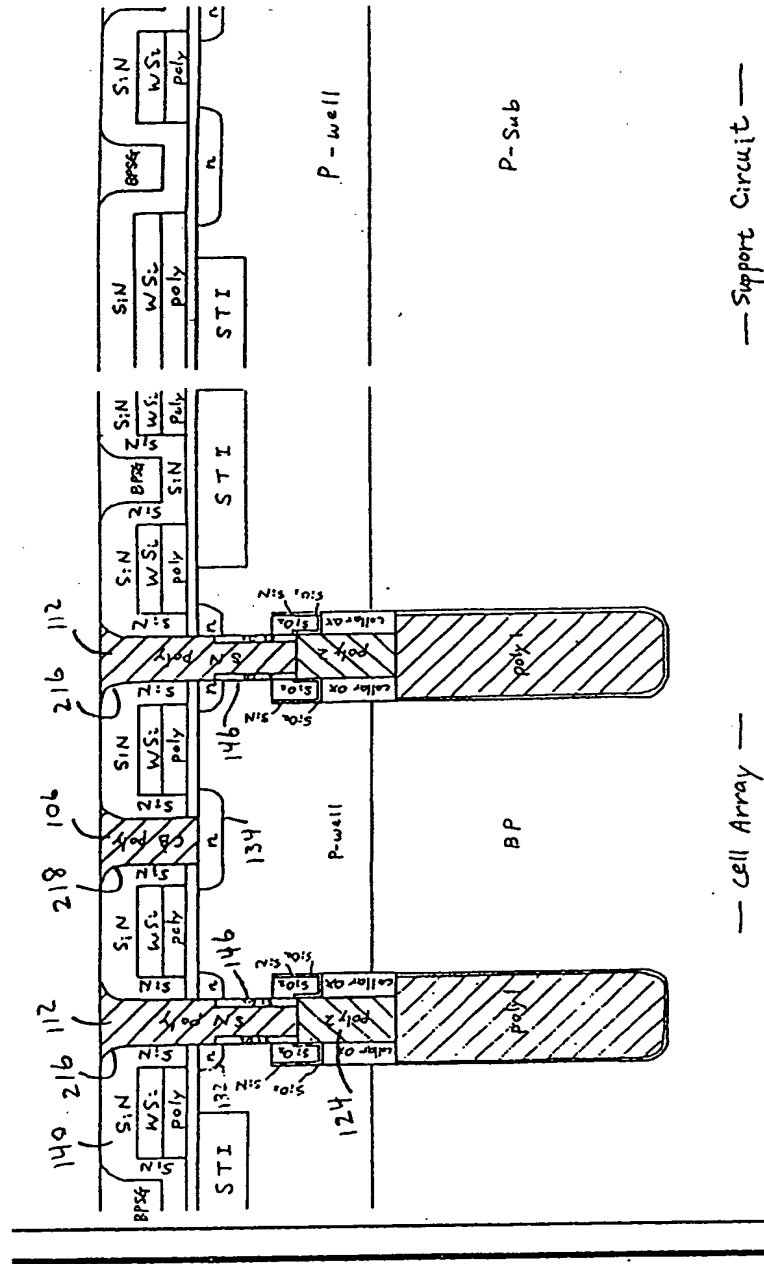
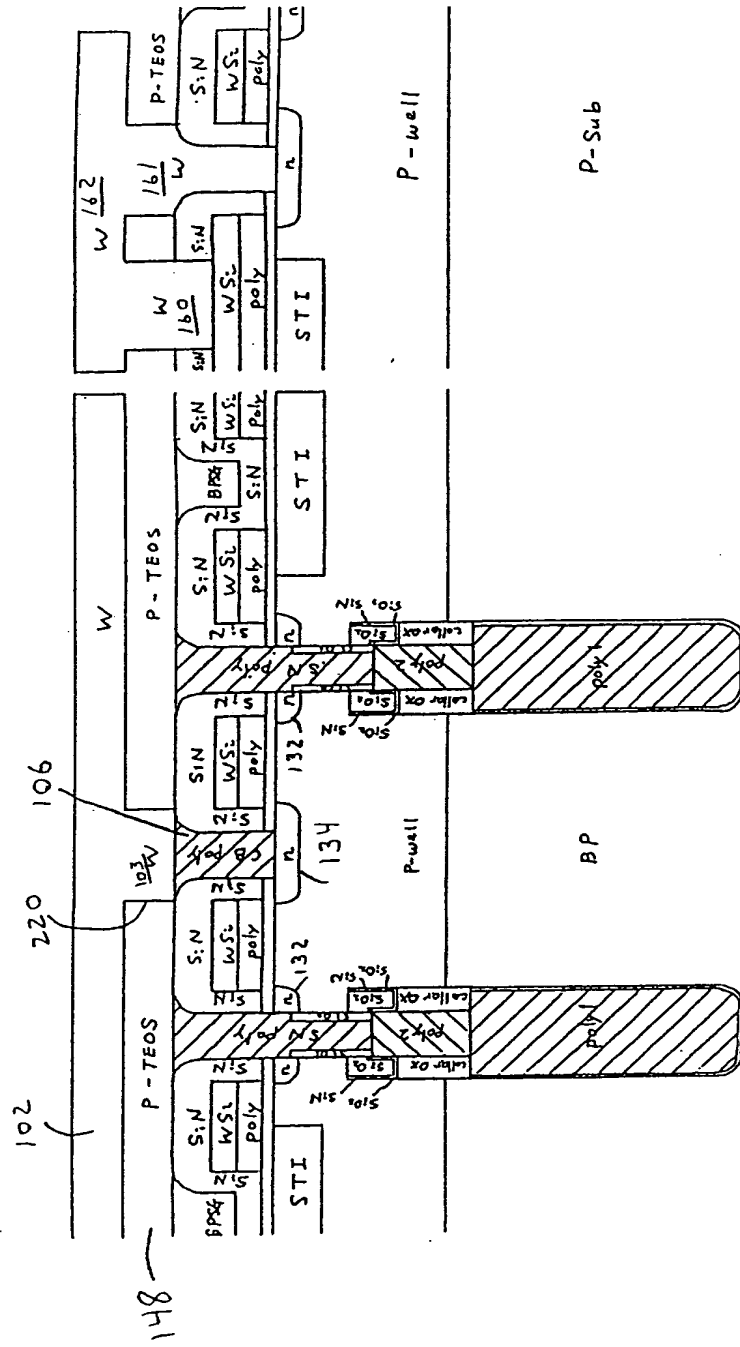


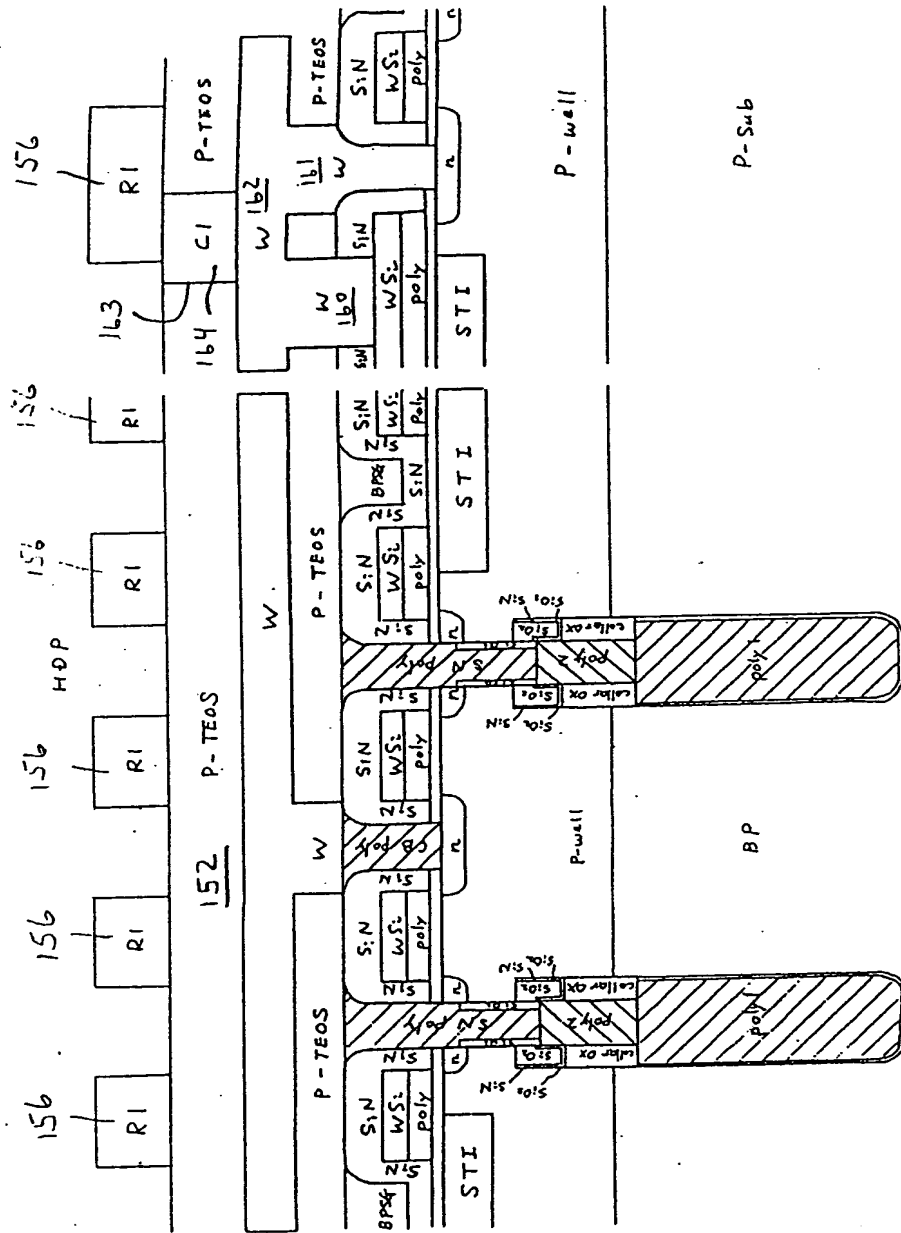
Figure 5I



— cell Array —

— Support Circuit —

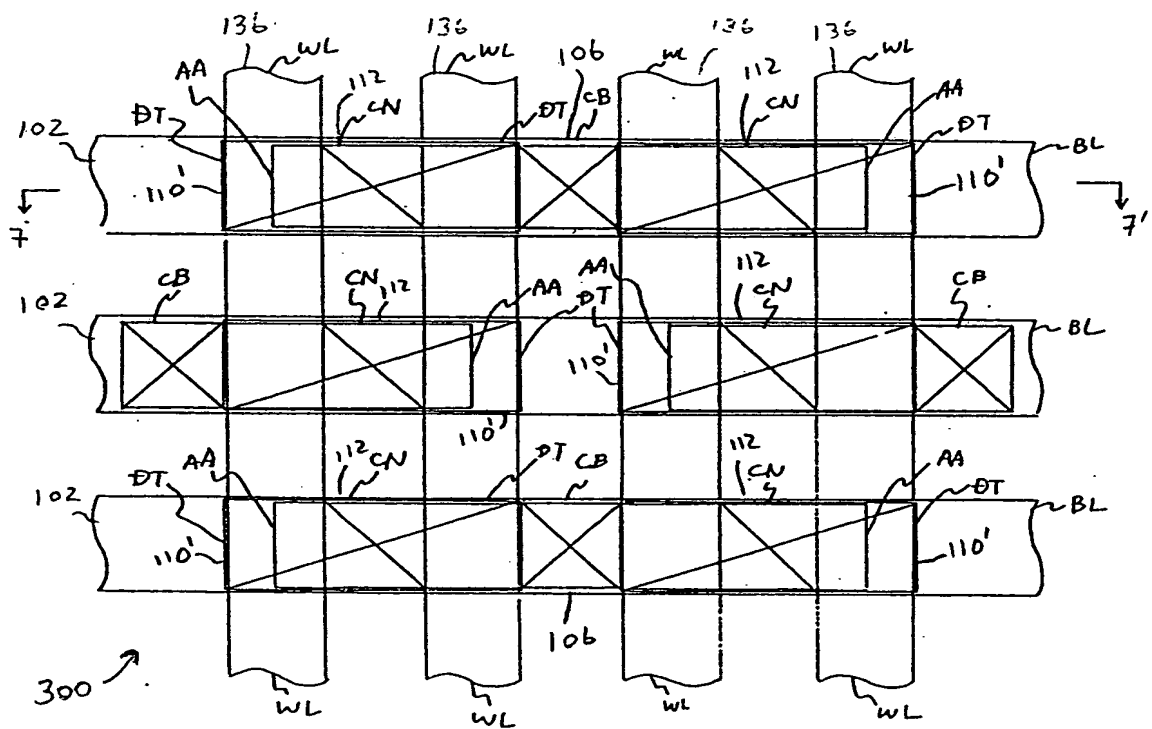
Figure 5J



—Cell Array —

—Support Circuit —

Figure 6





— Support Circuit —

Figure 8

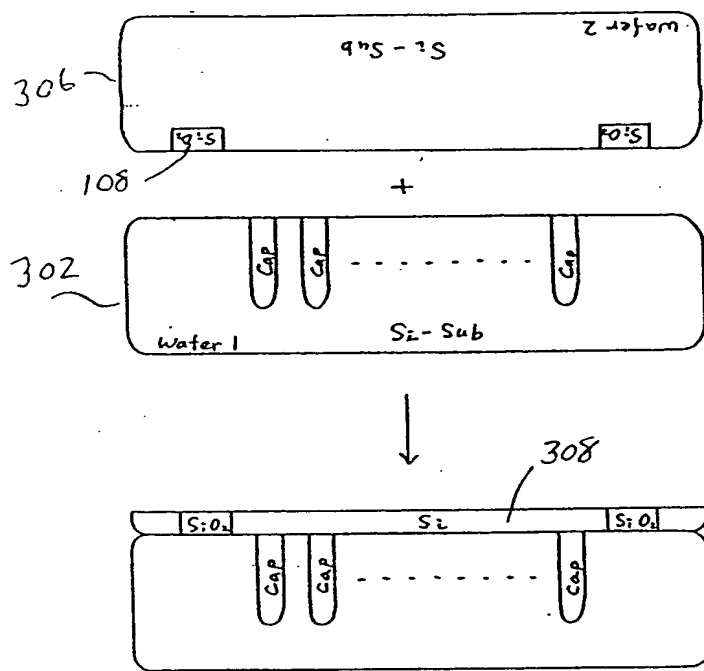


Figure 9A

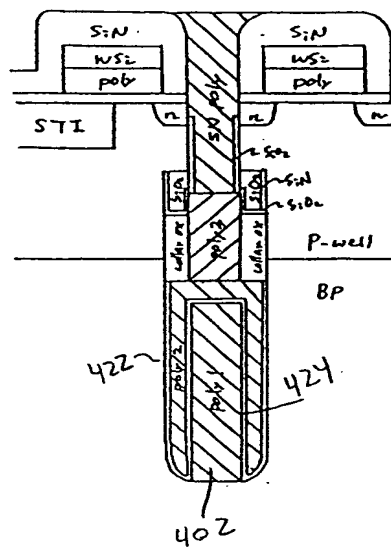
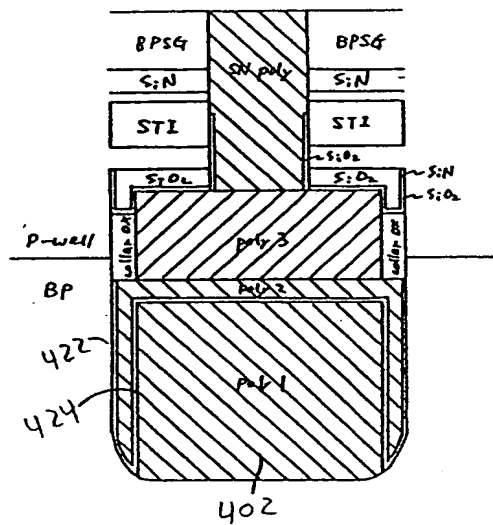


Figure 9B



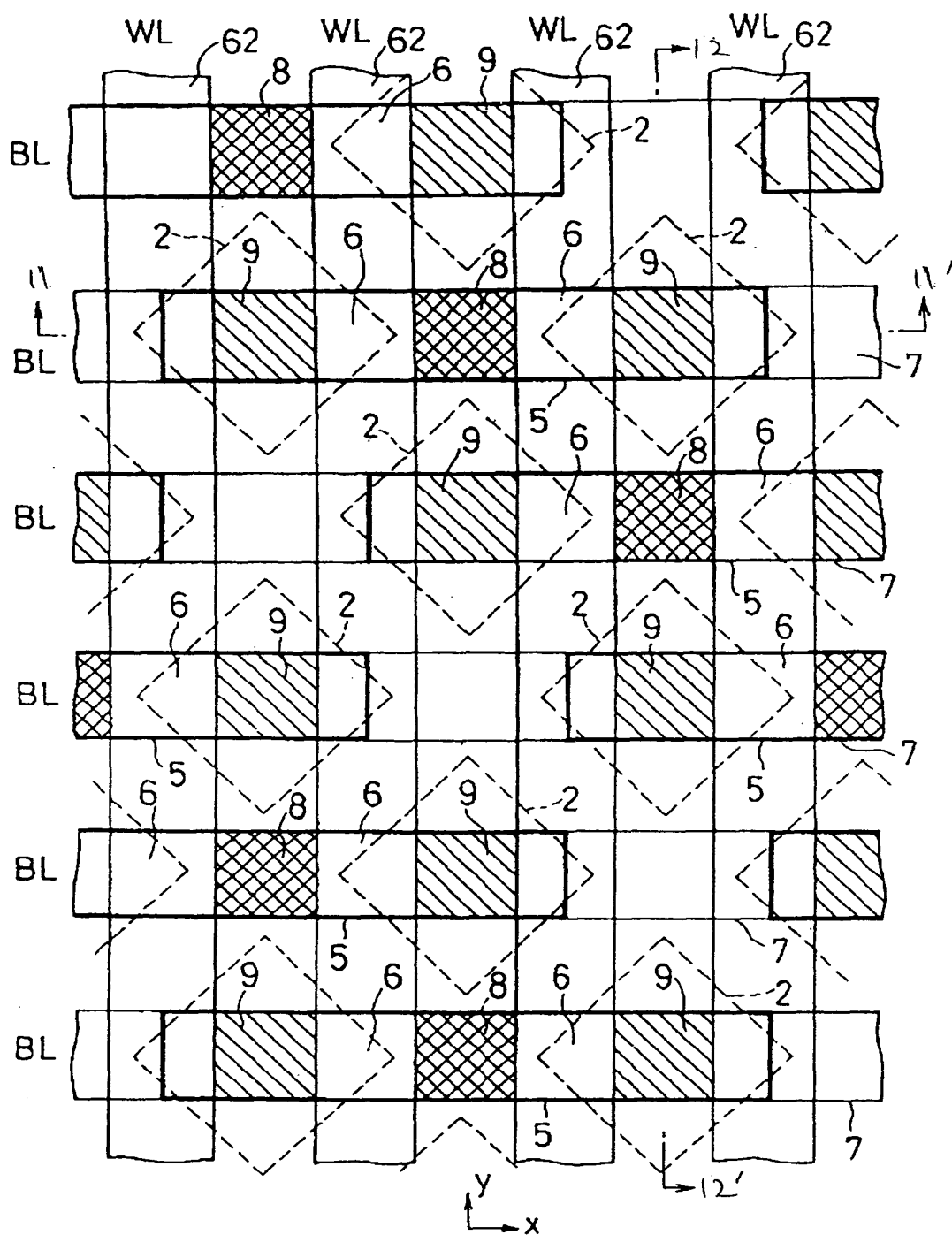


Figure 10

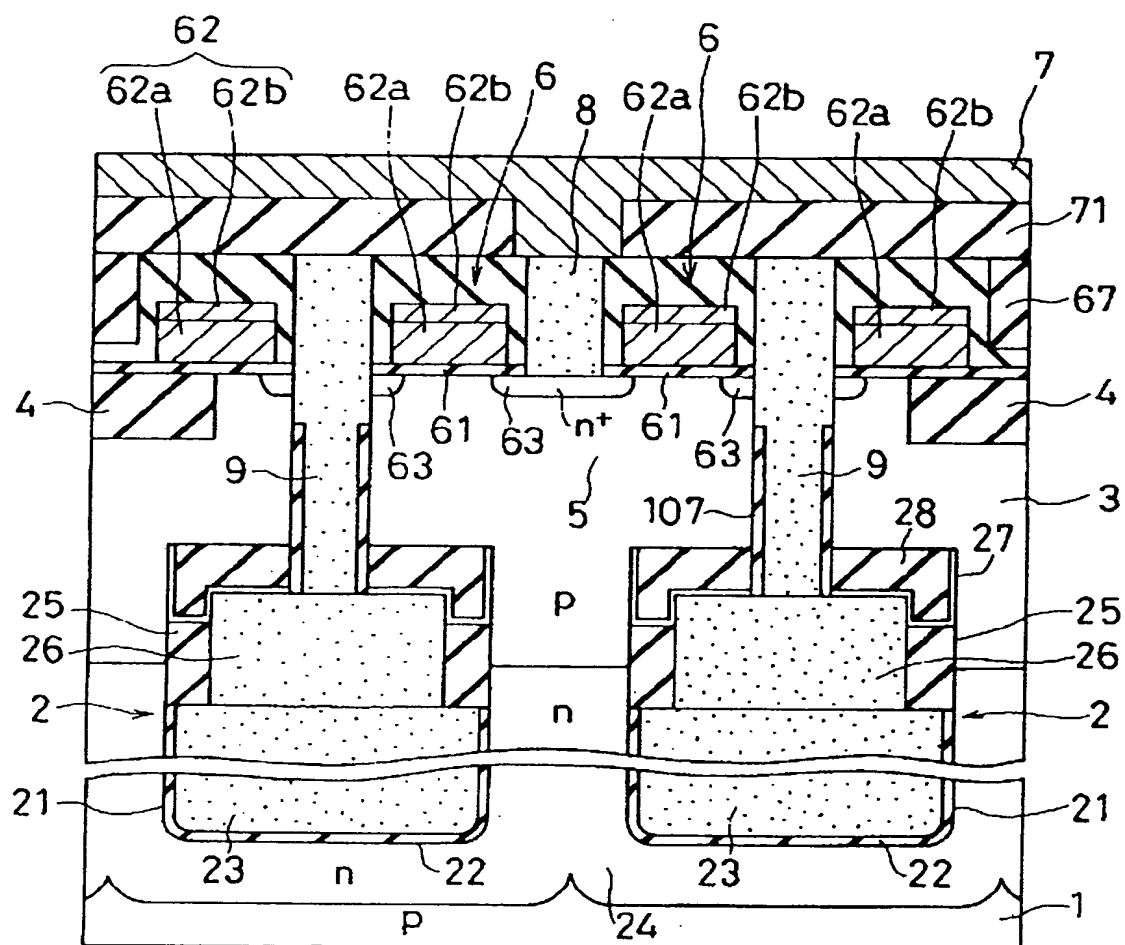


Figure 11

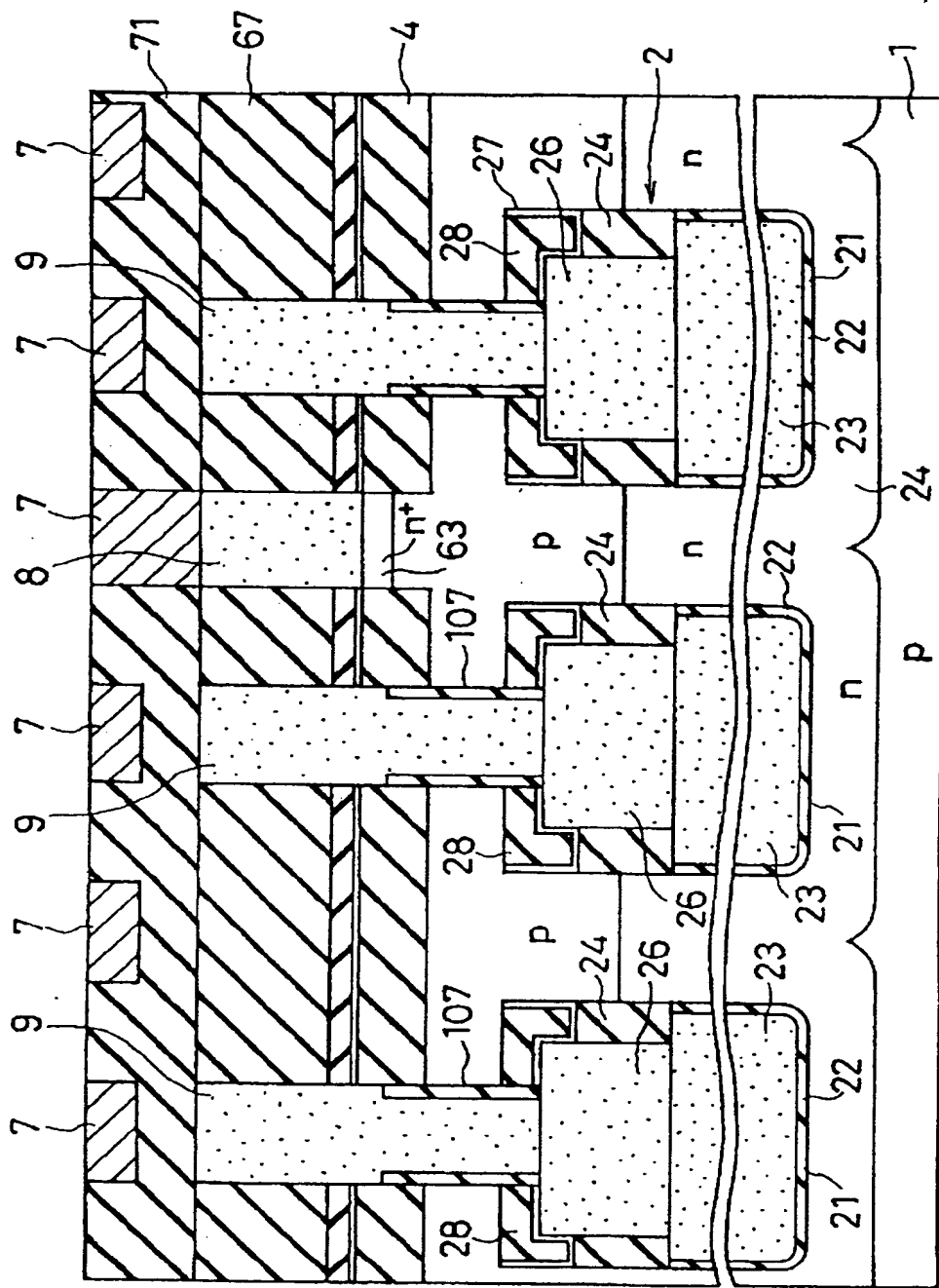


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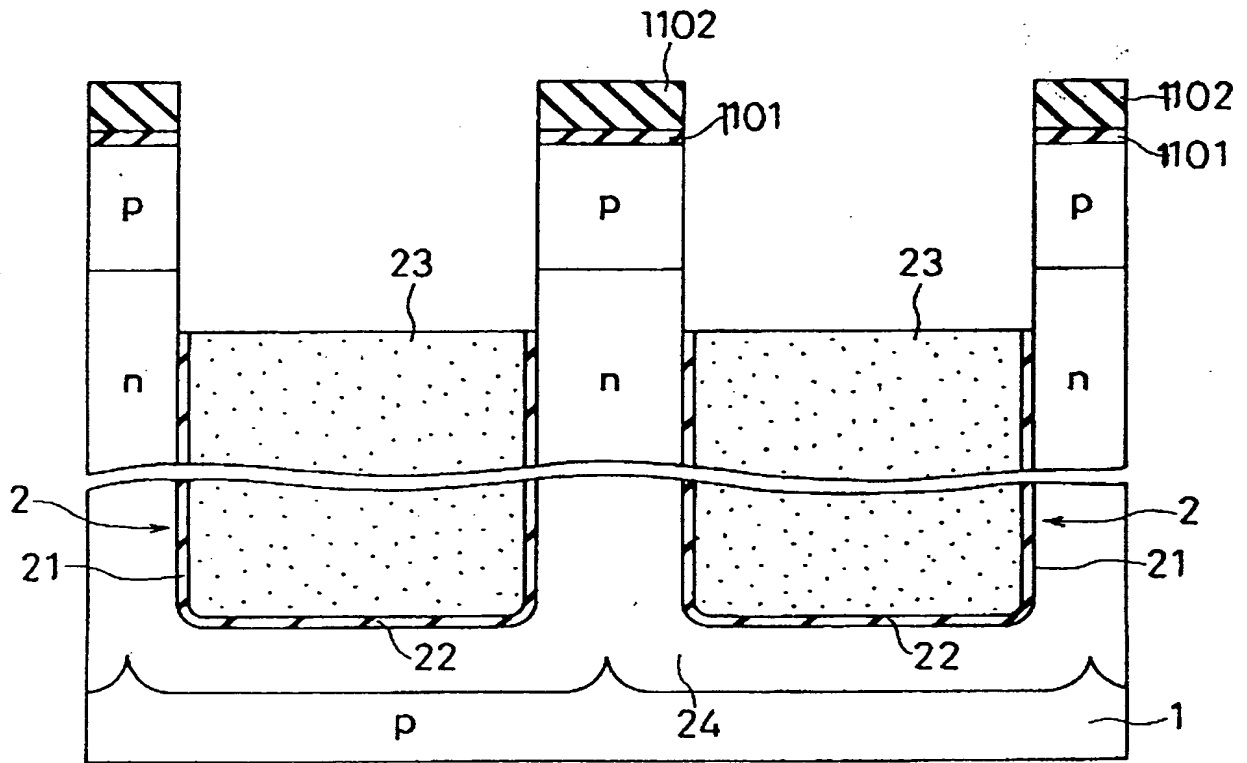


Figure 13A

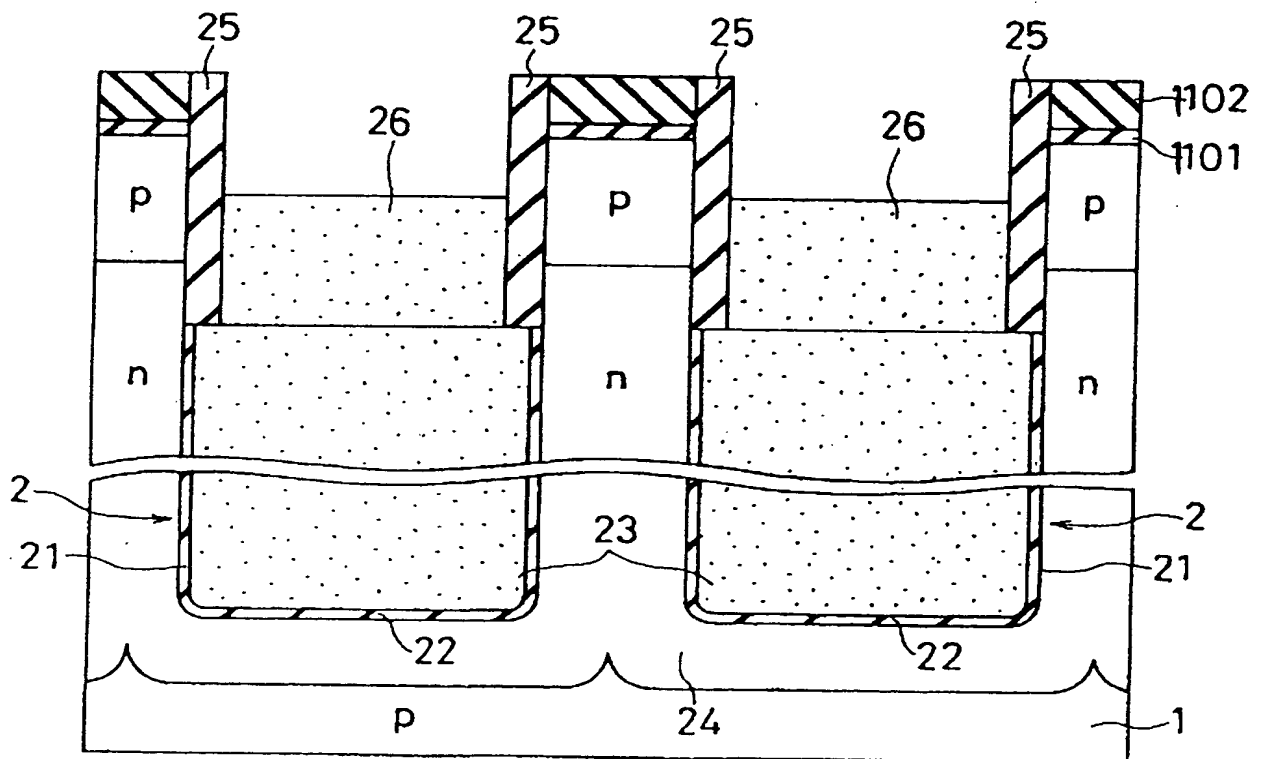


Figure 13B

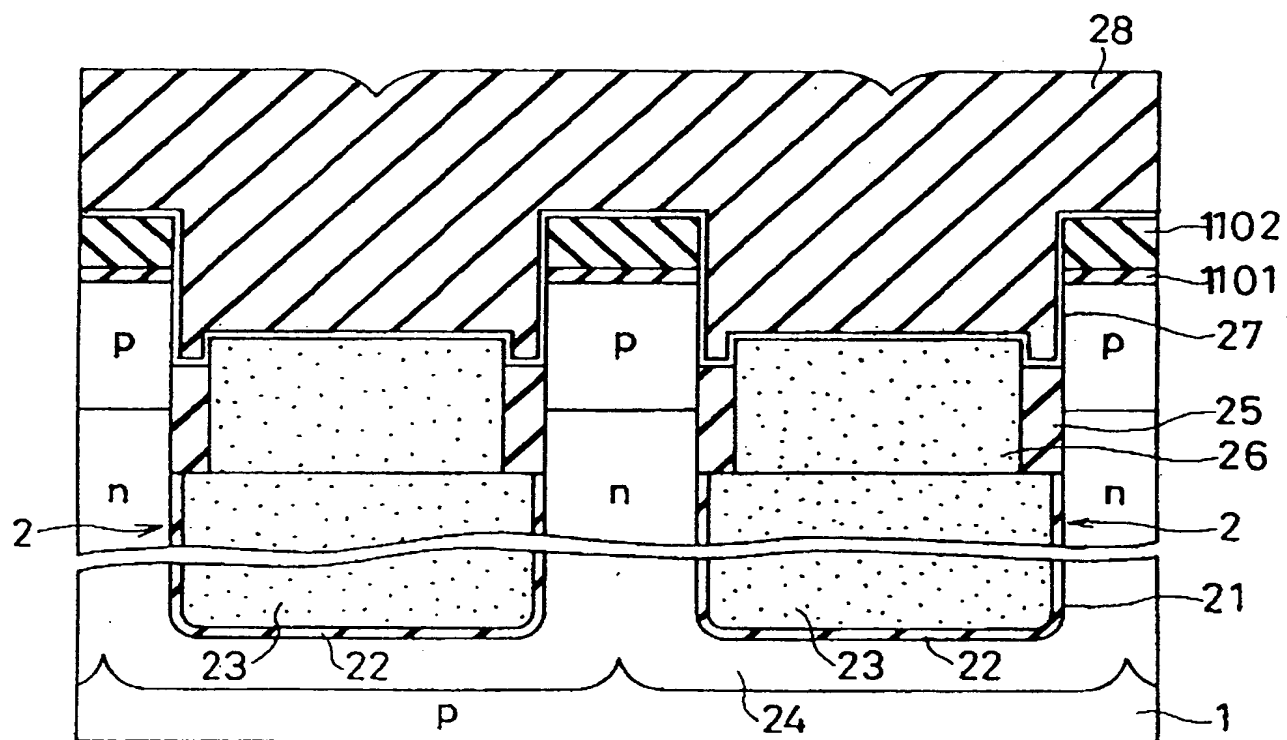


Figure 13C

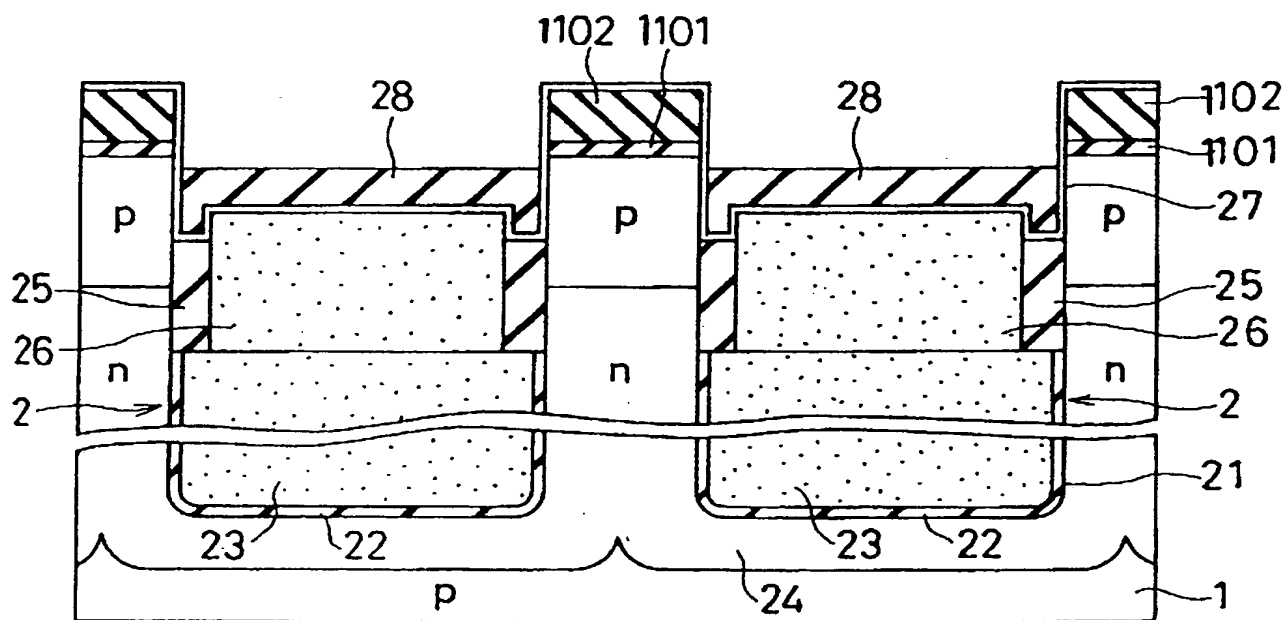


Figure 13-D



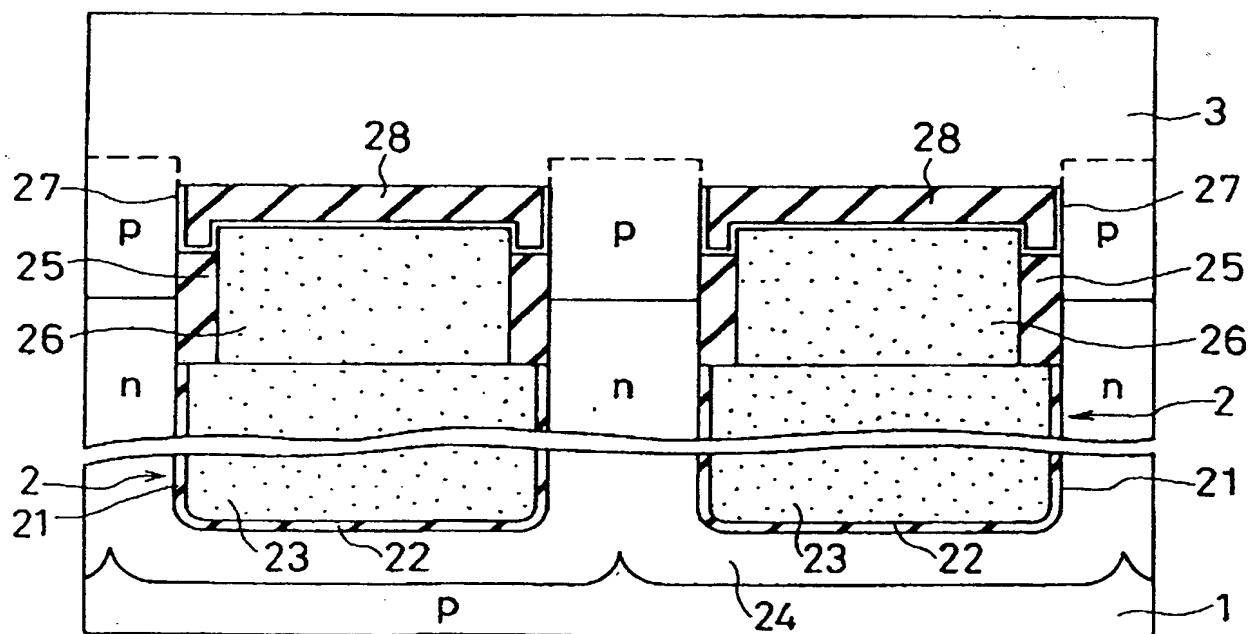


Figure 13E

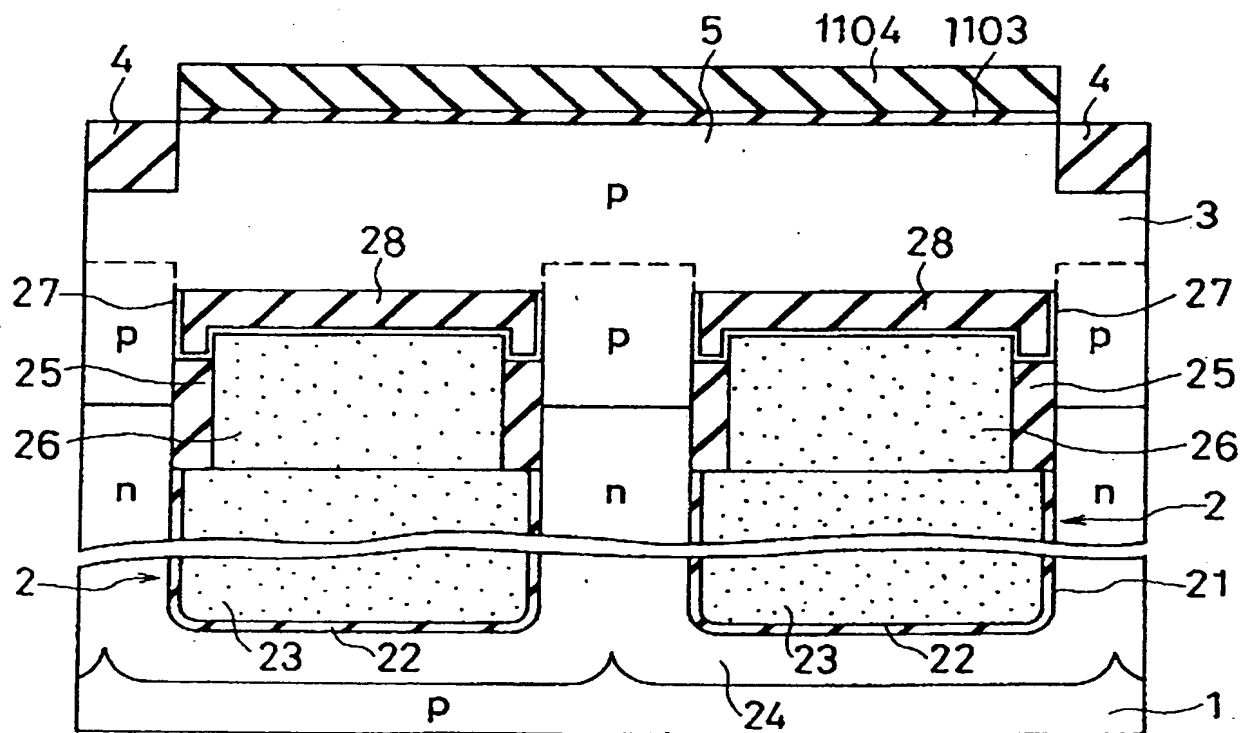


Figure 13 F

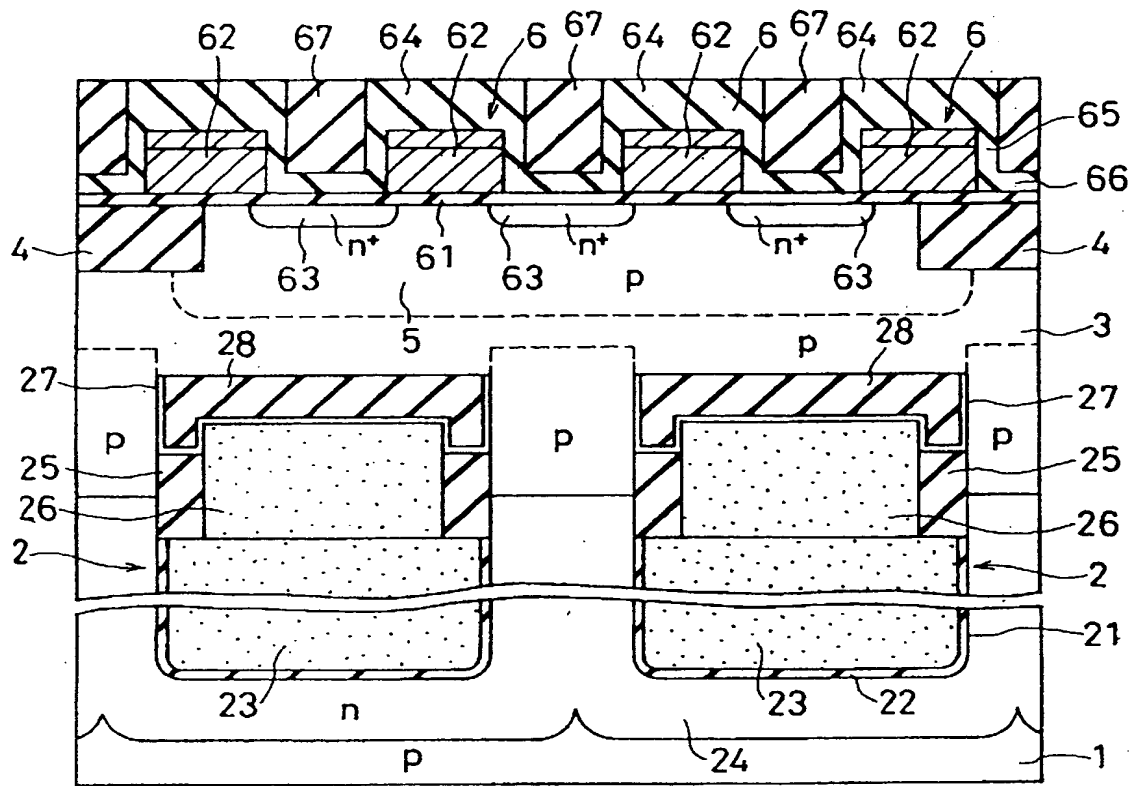


Figure 13G

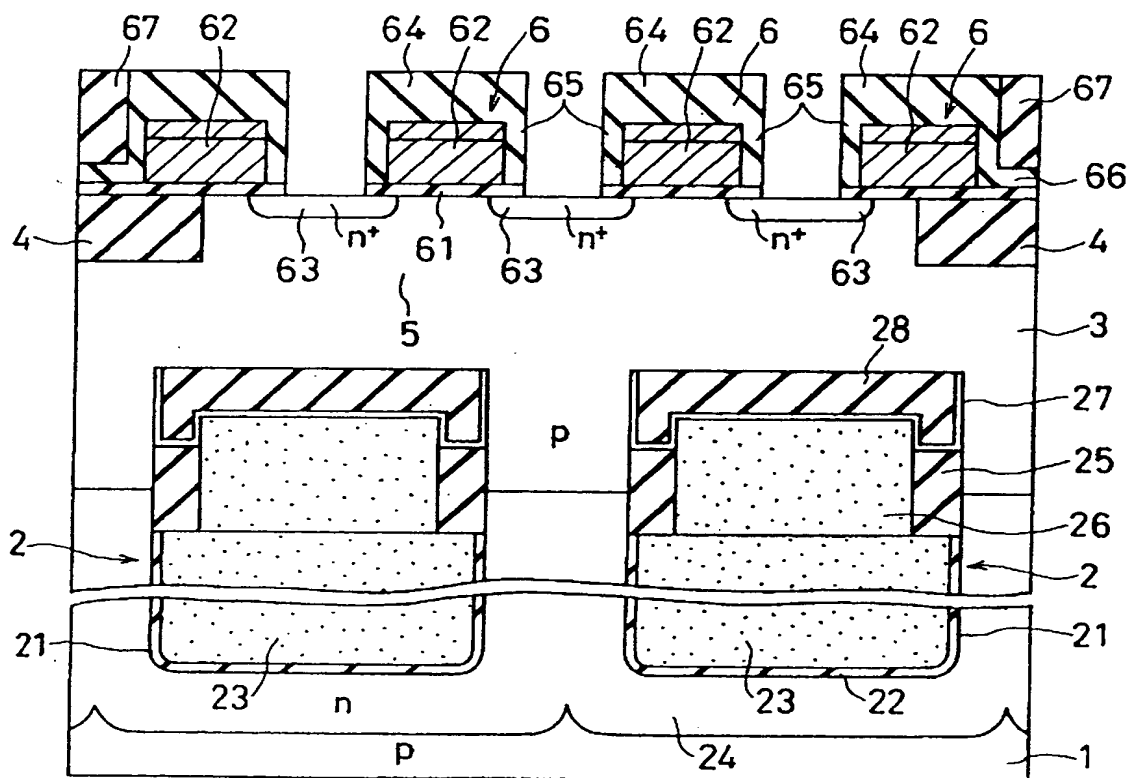


Figure 13H

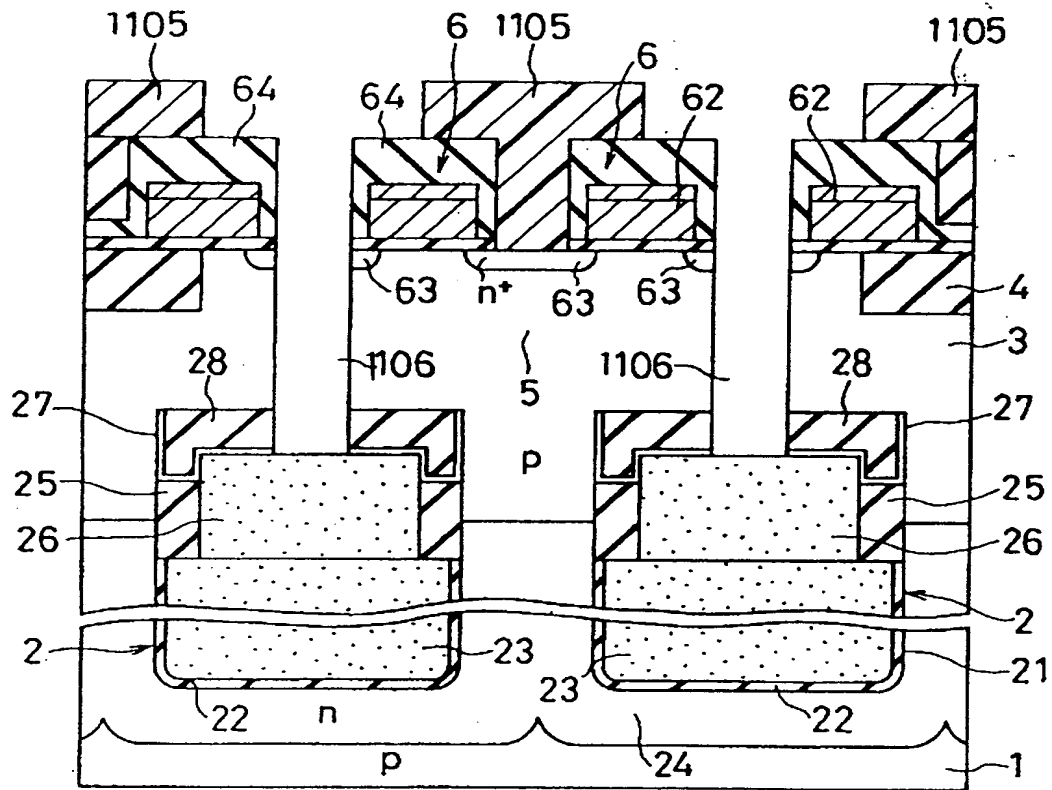


Figure 13I

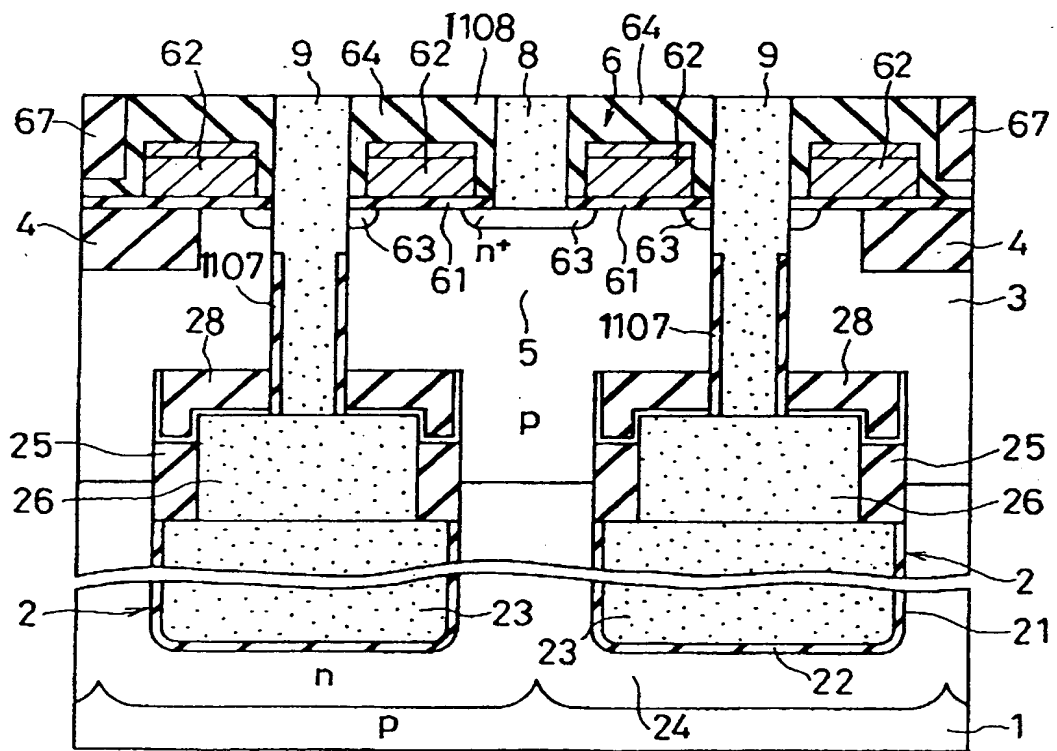


Figure 13J

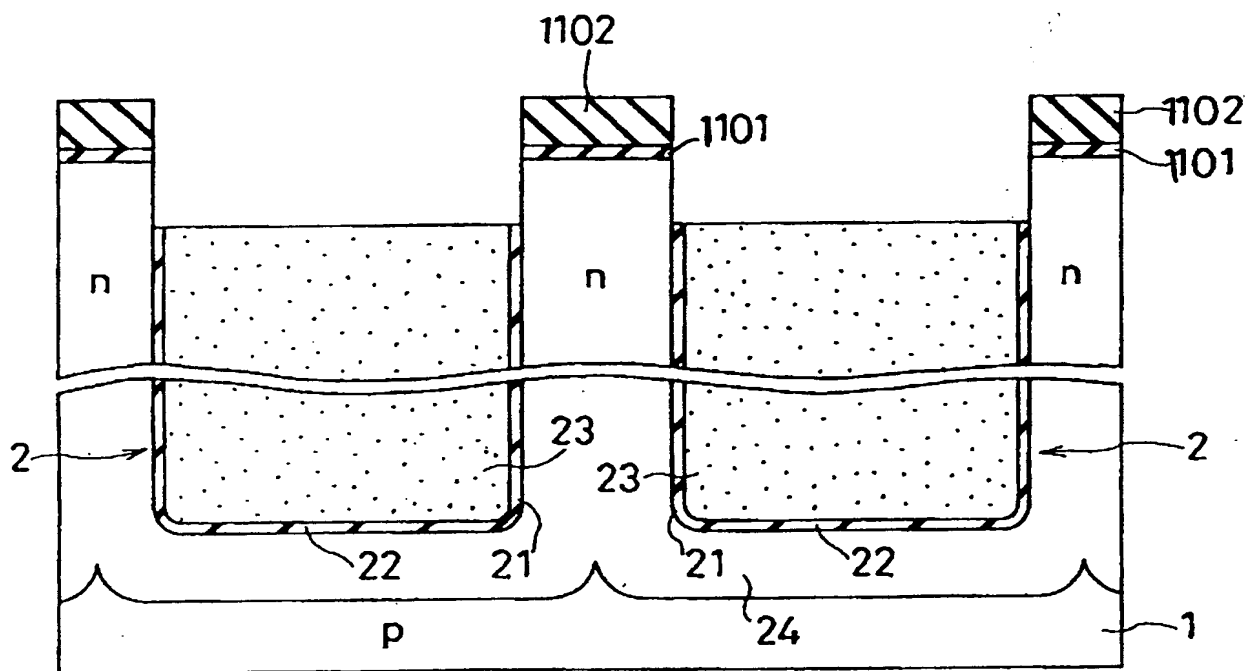


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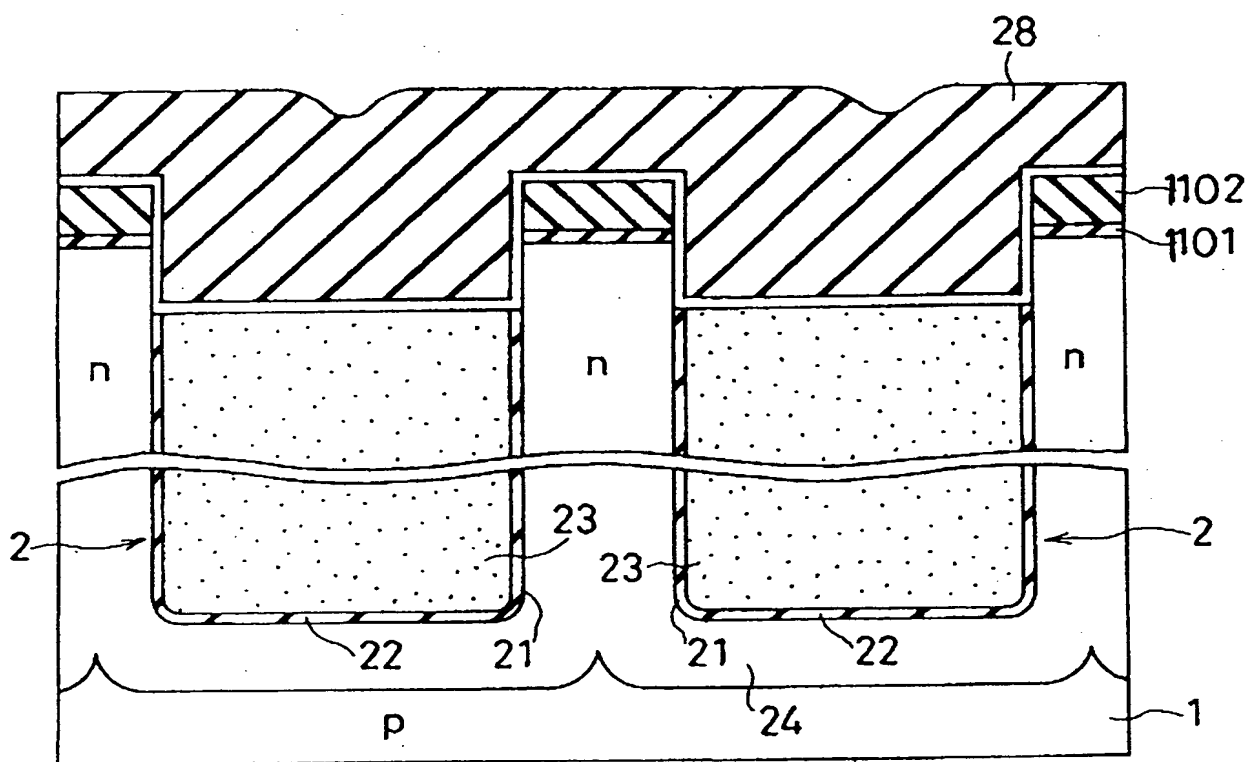
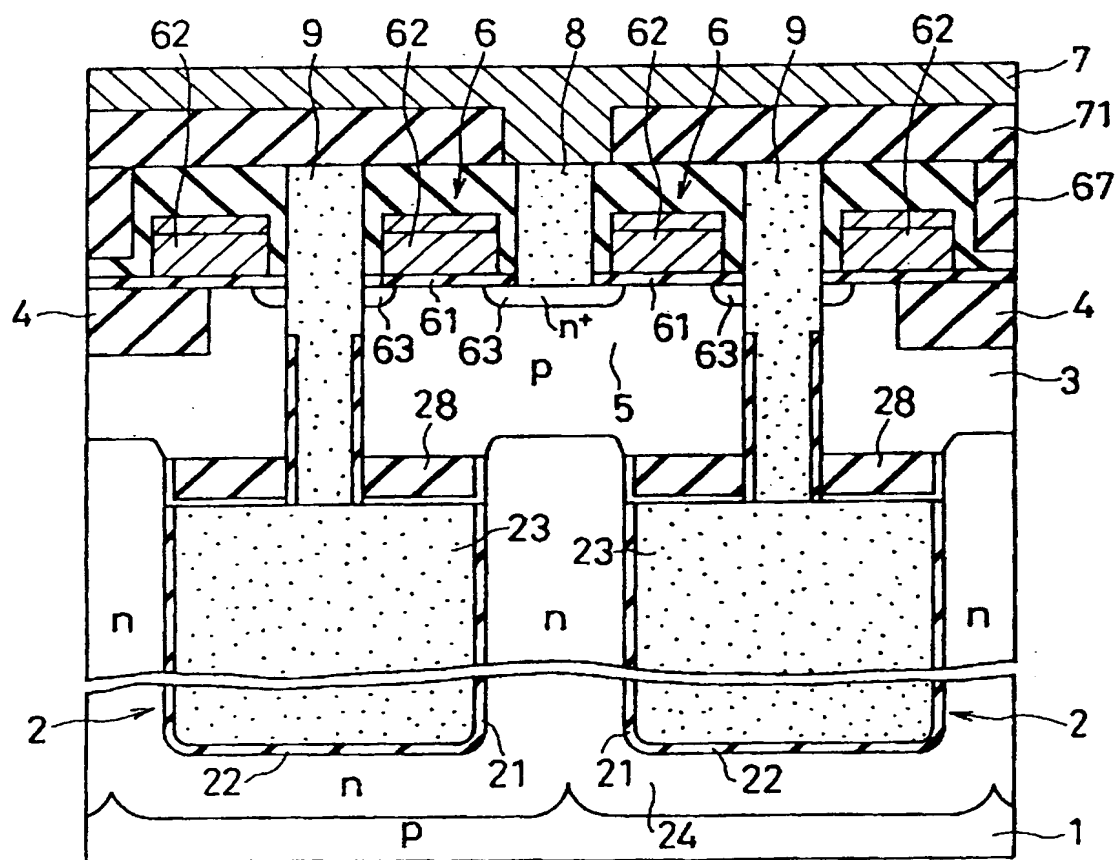
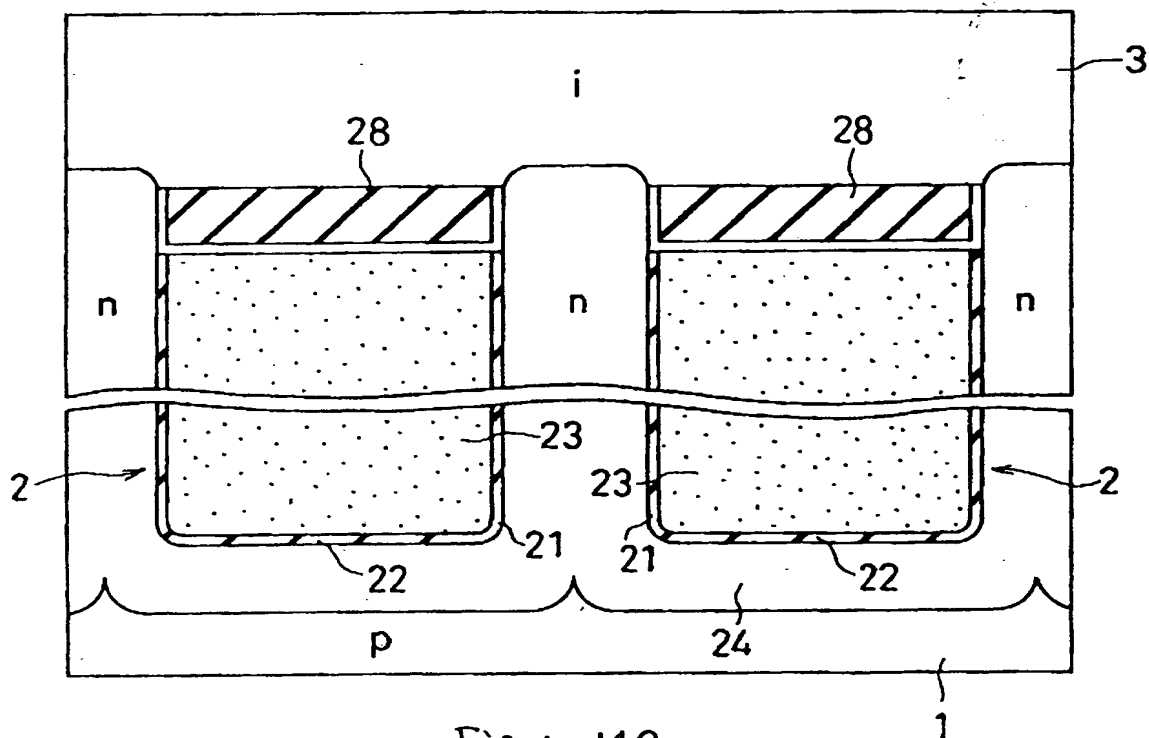


Figure 14B



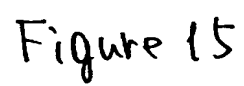


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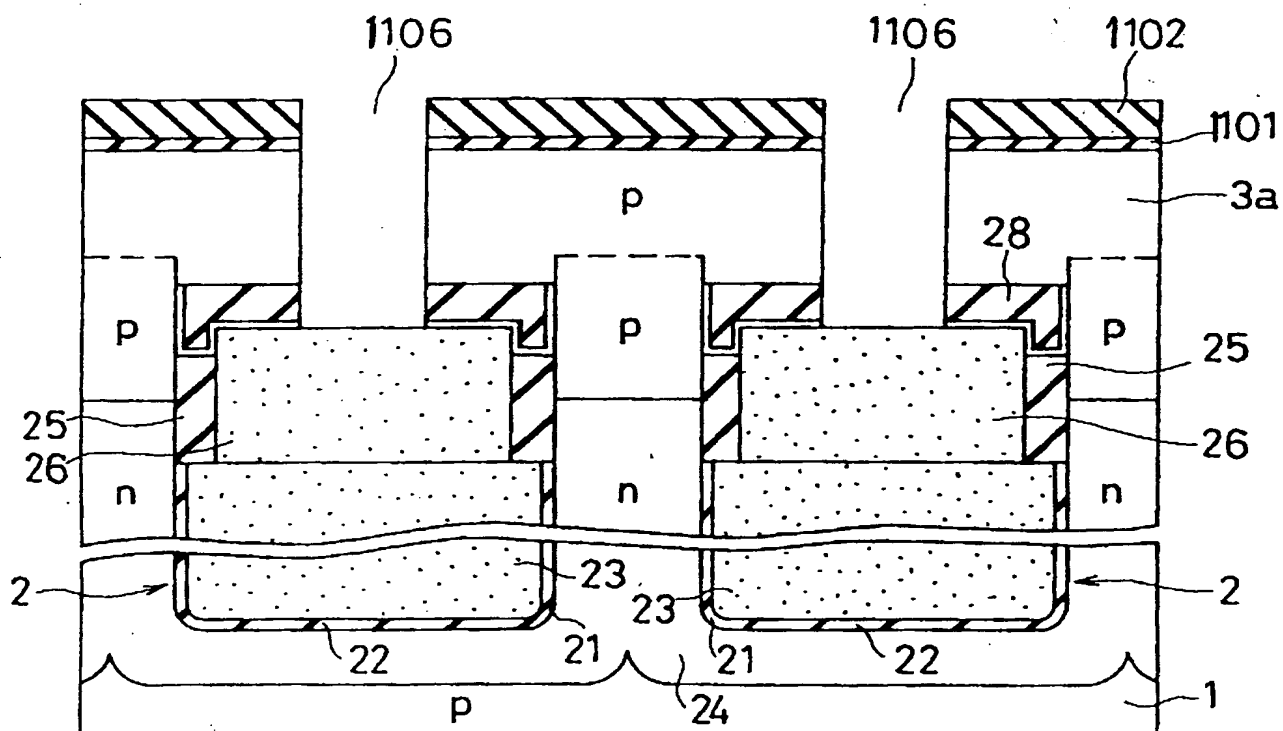


Figure 16A

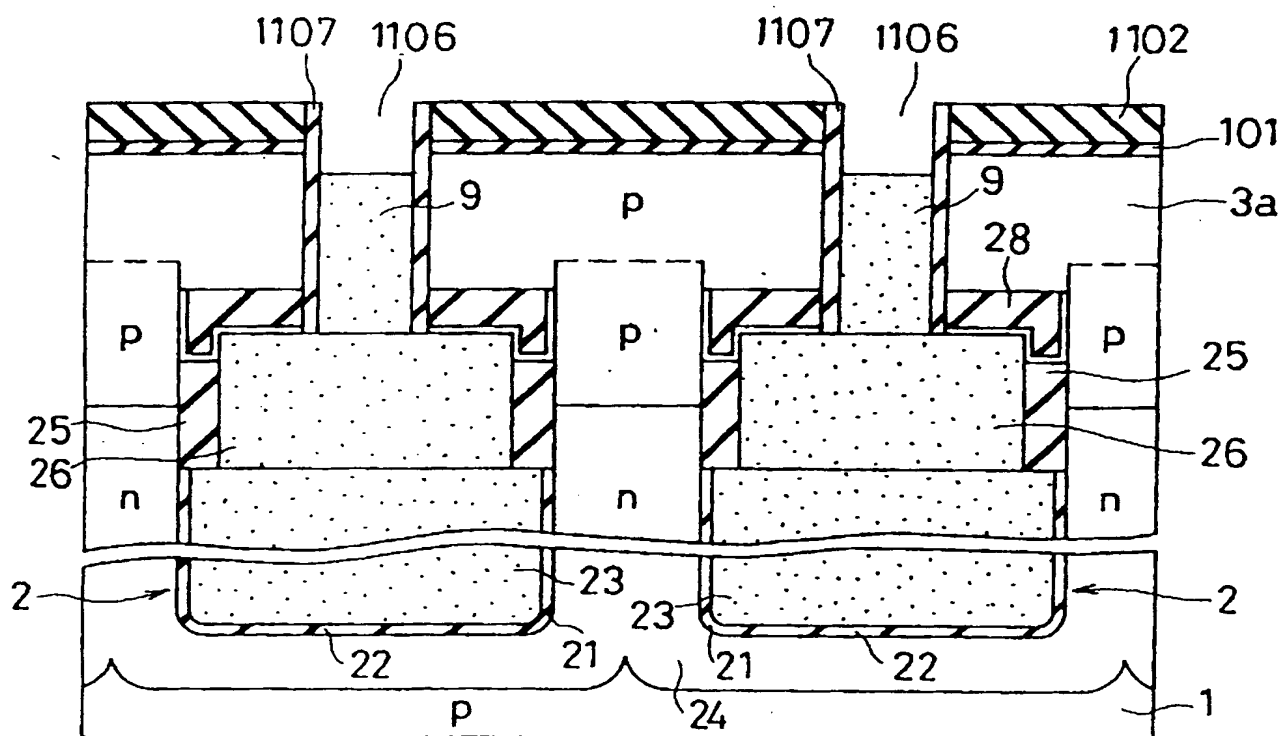


Figure 16B

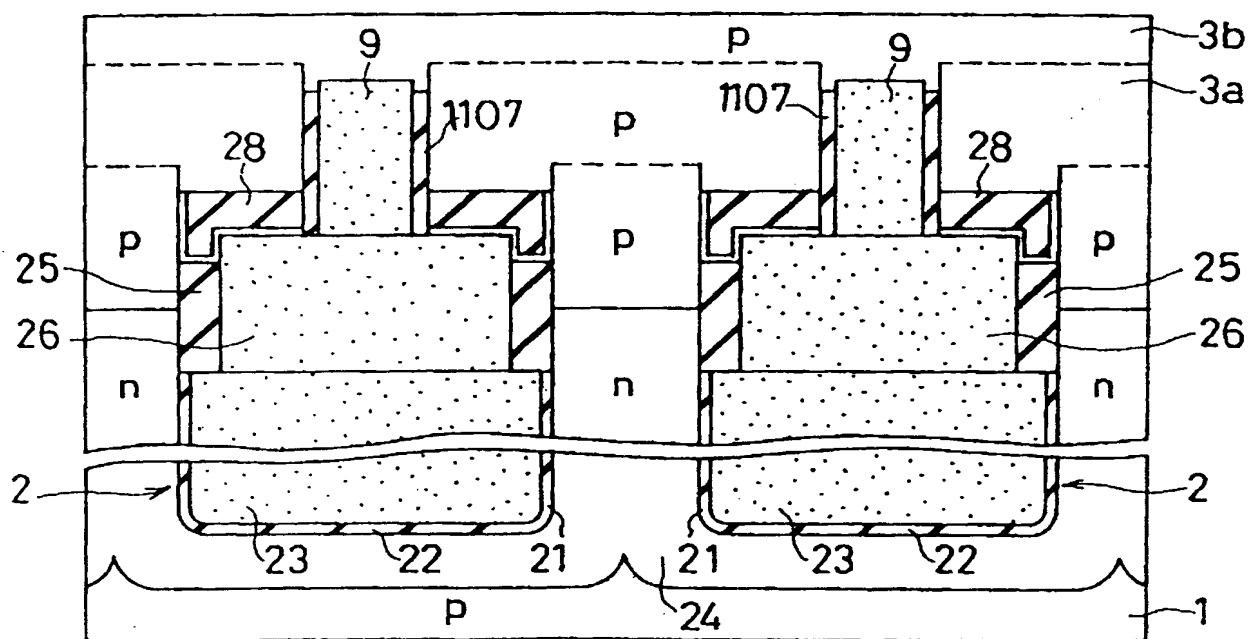


Figure 16C

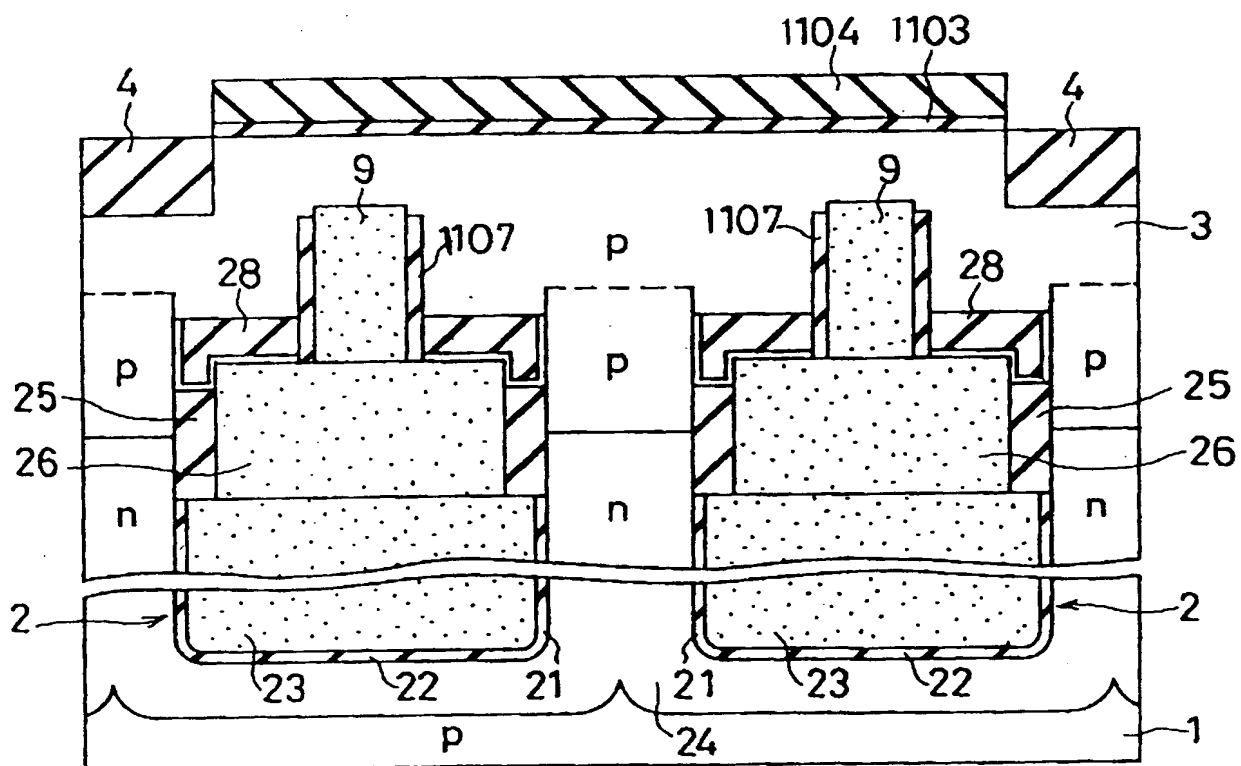


Figure 16D



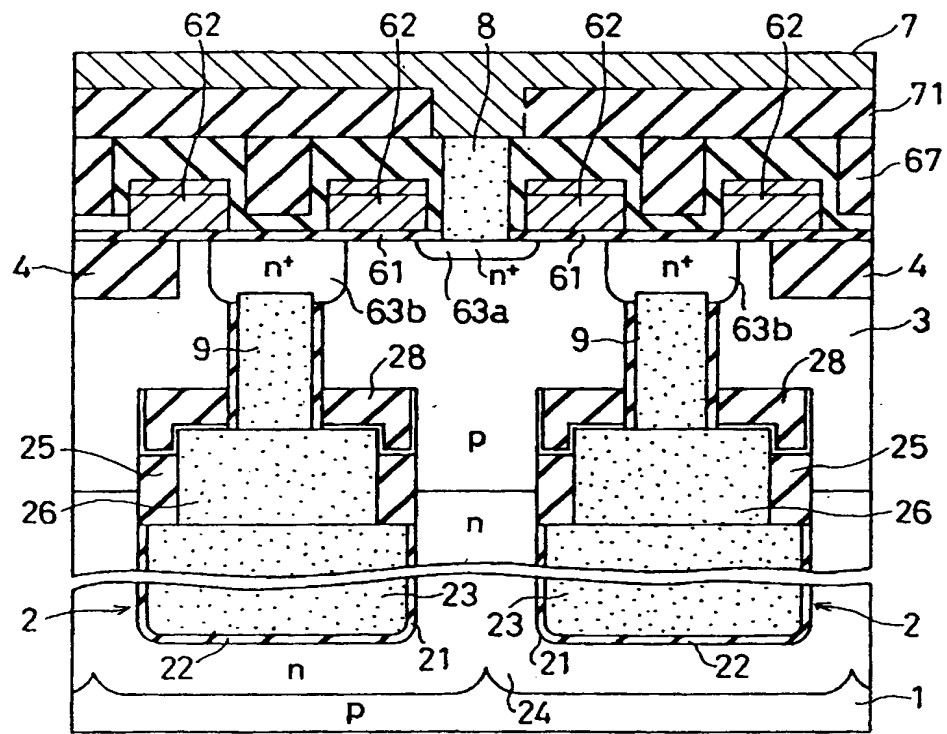


Figure 16E

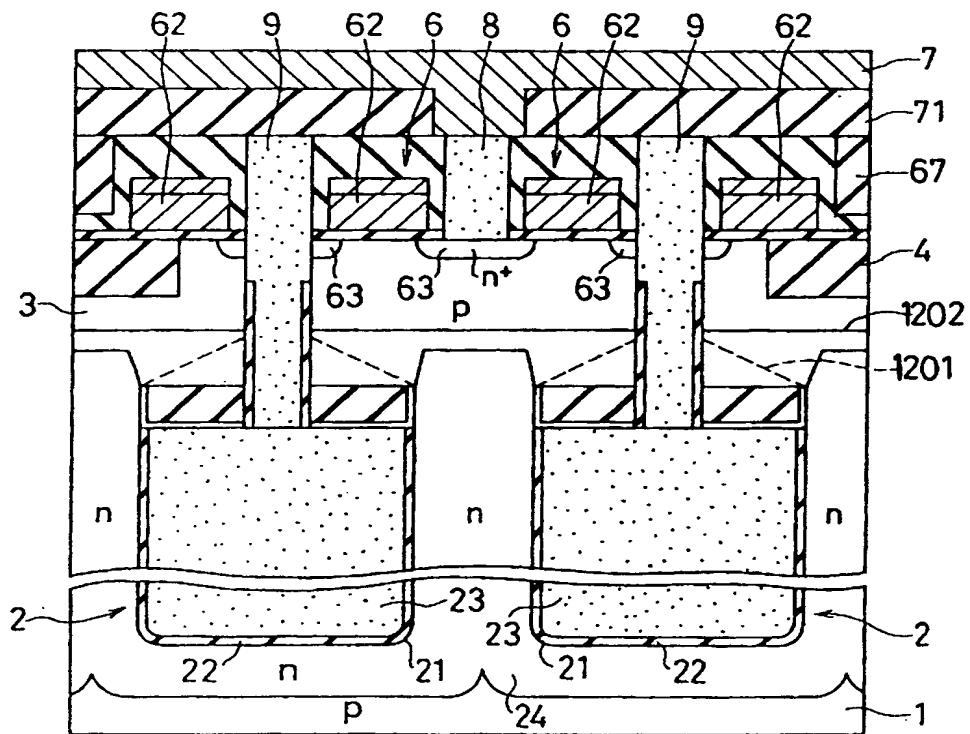


Figure 17

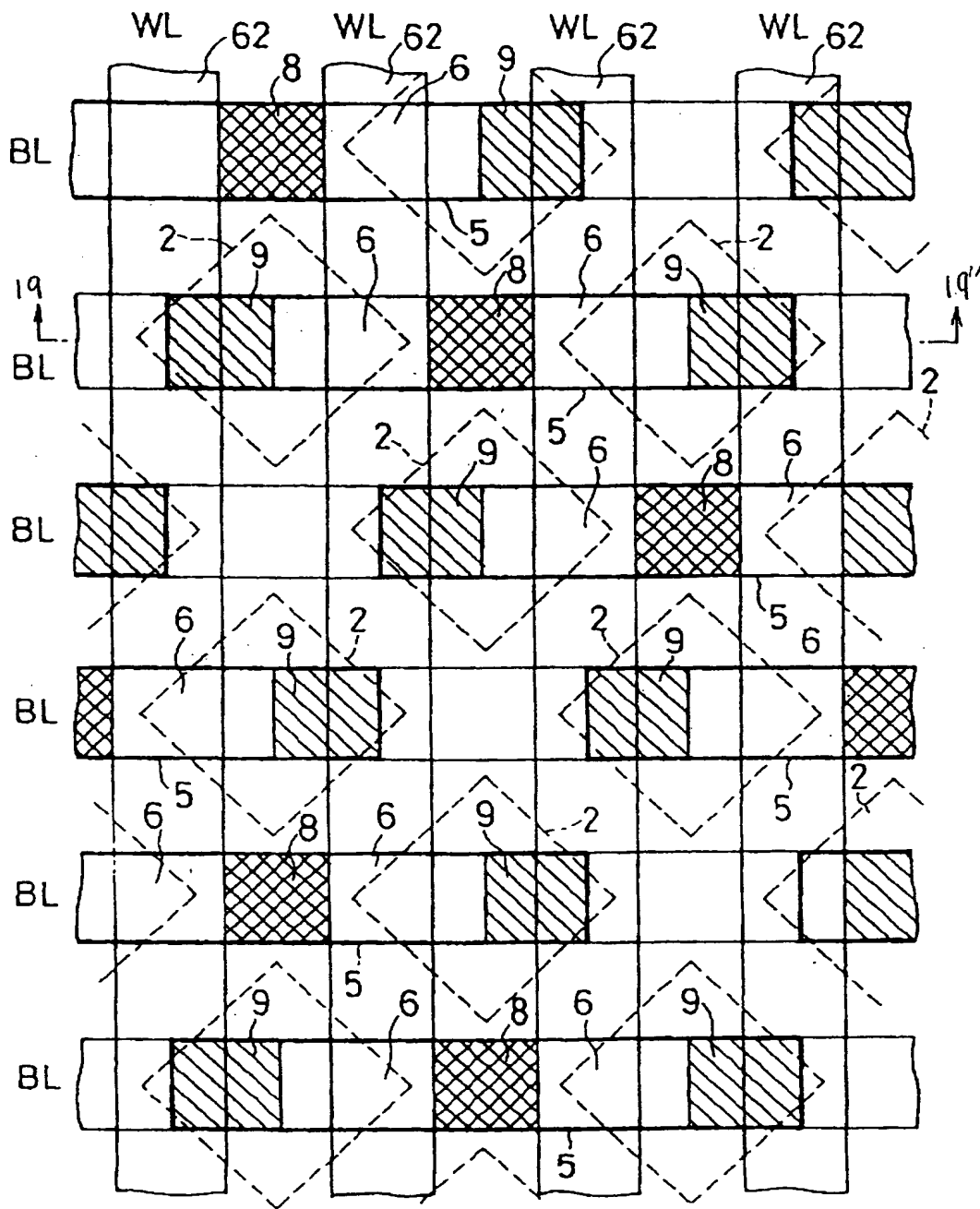


Figure 18

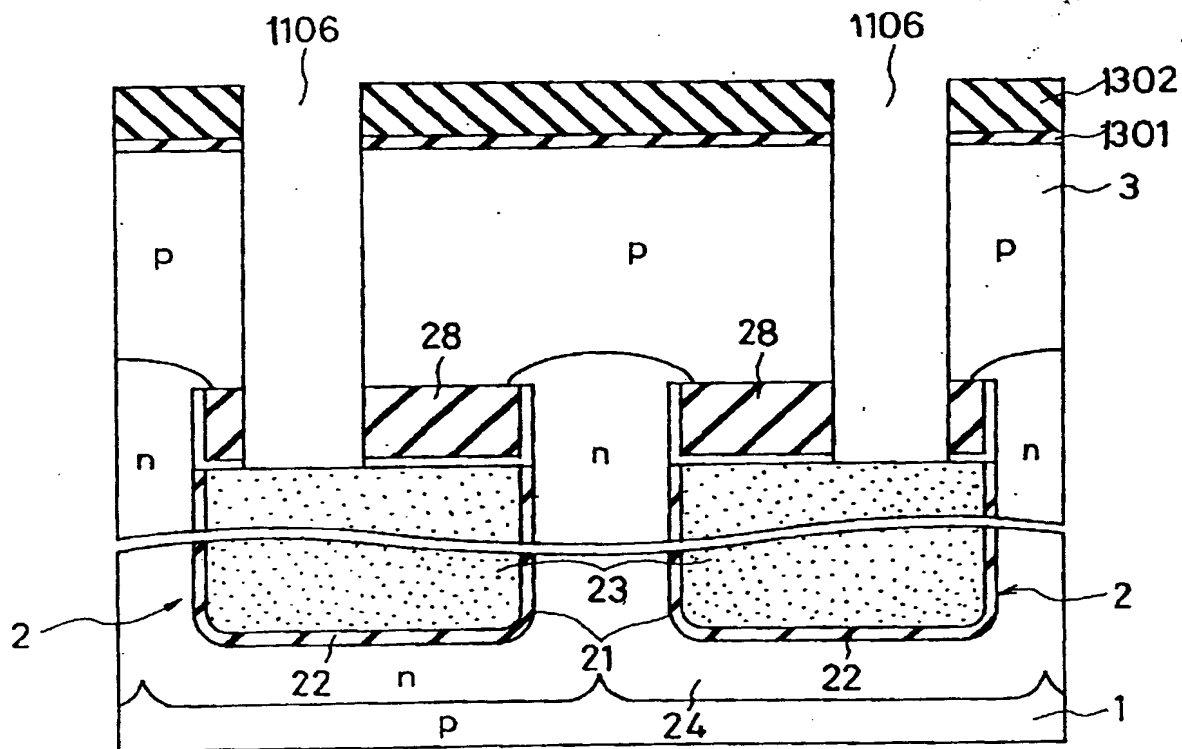


Figure 19A

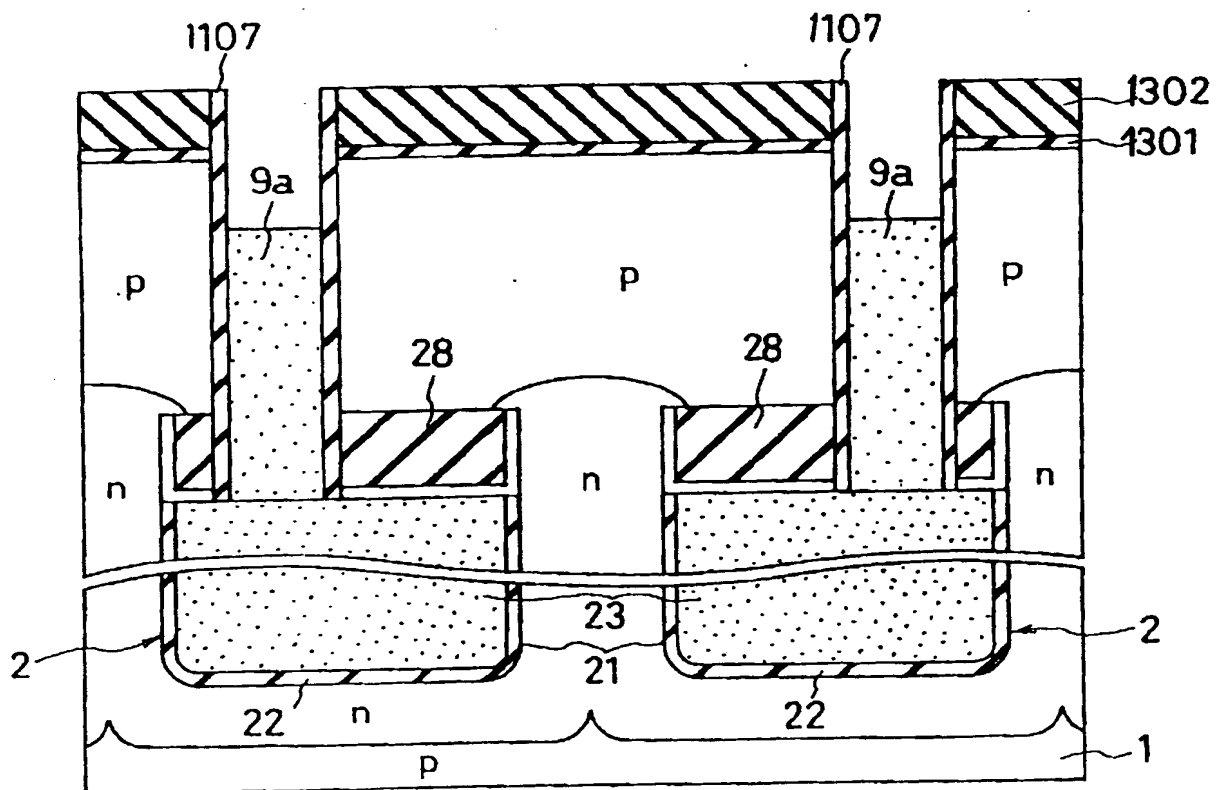


Figure 19B

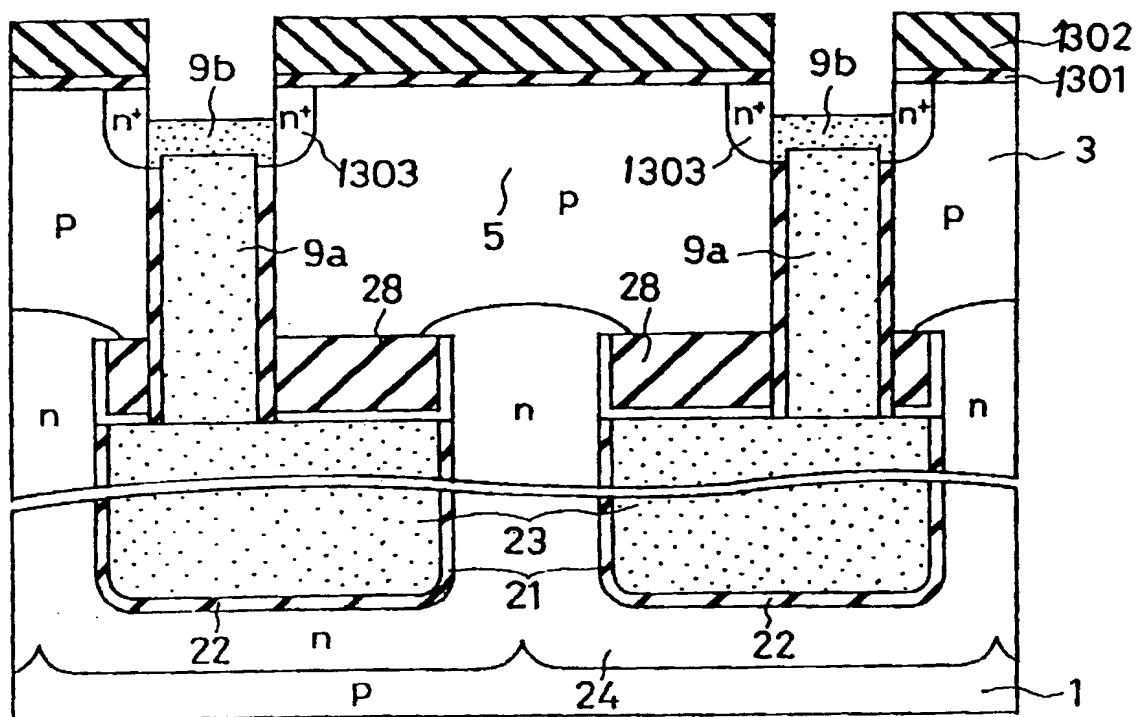


Figure 19c

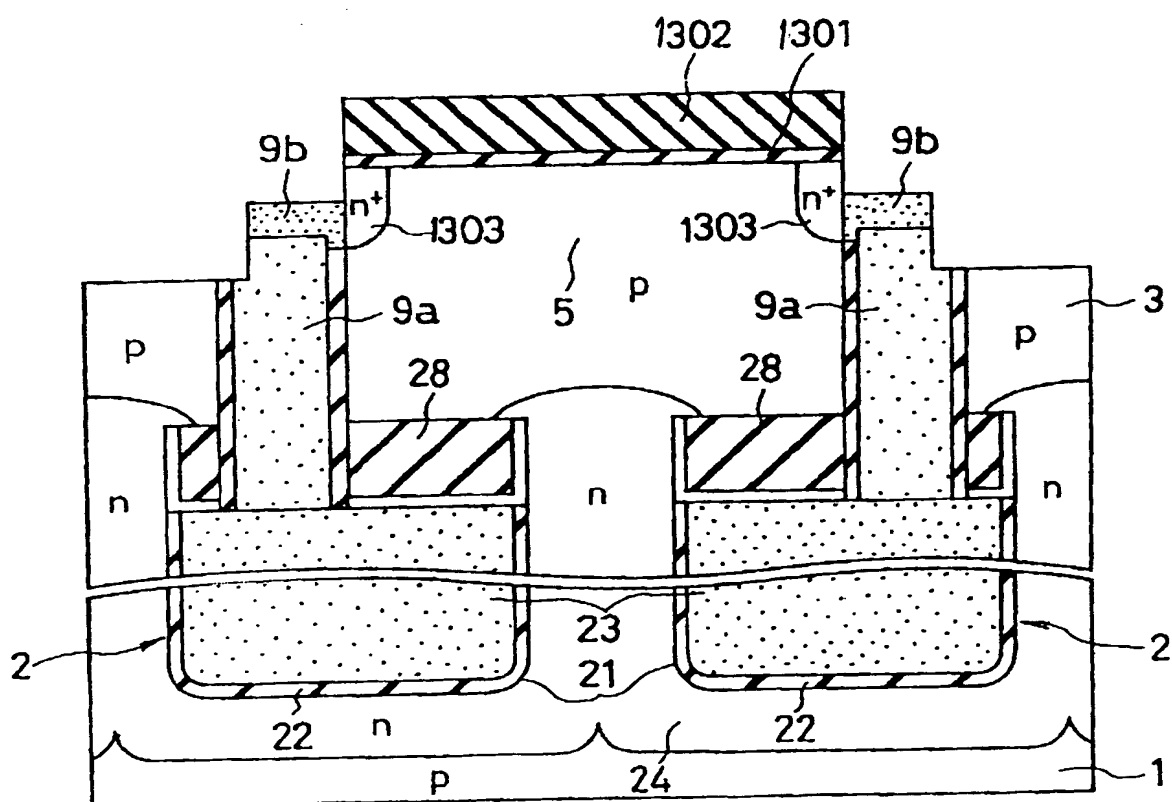


Figure 19D

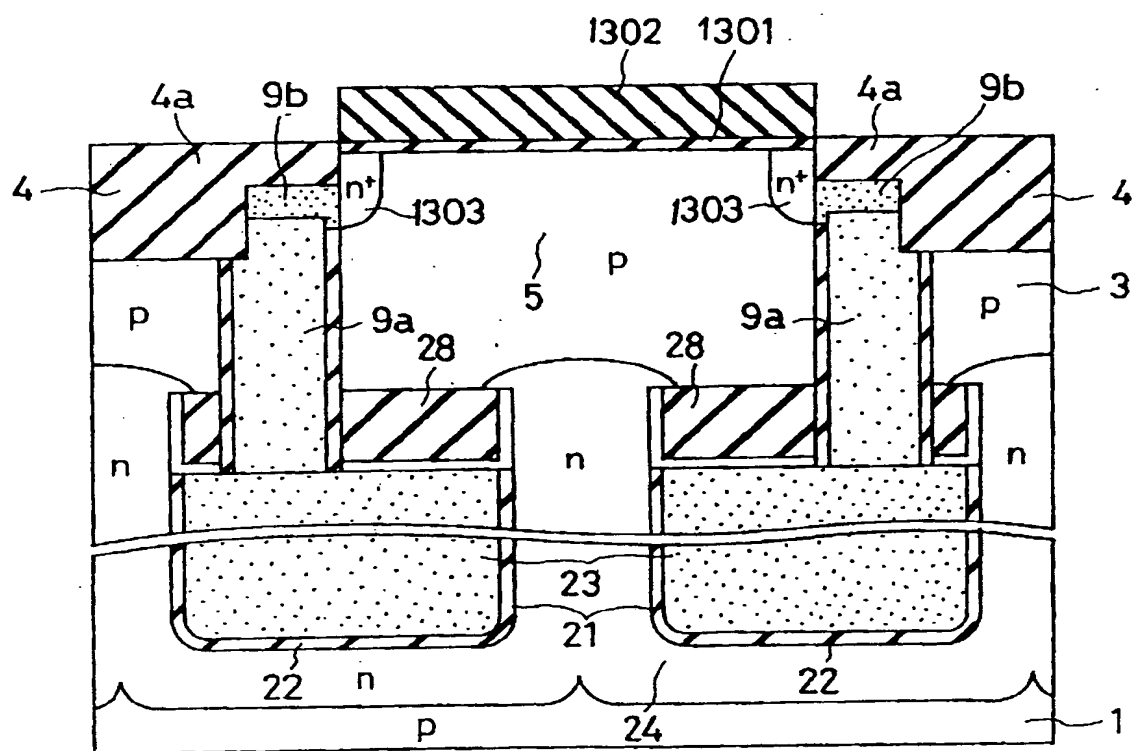


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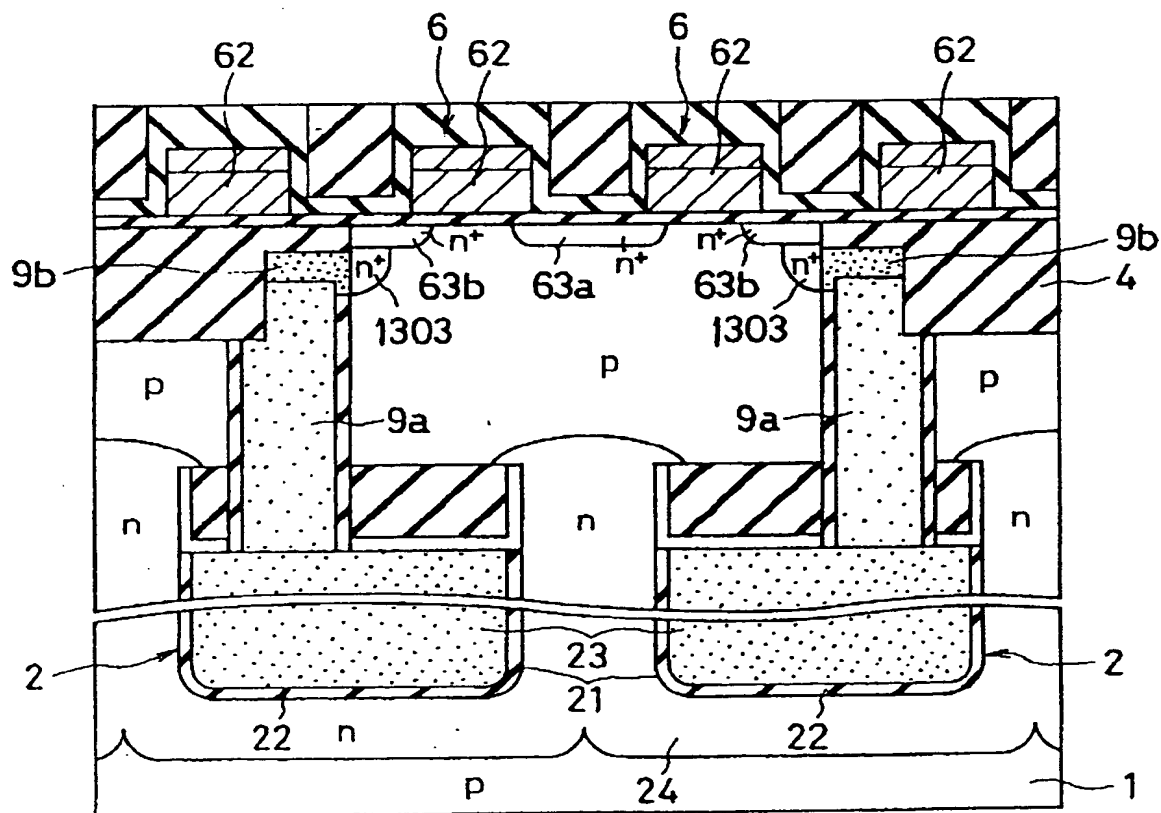


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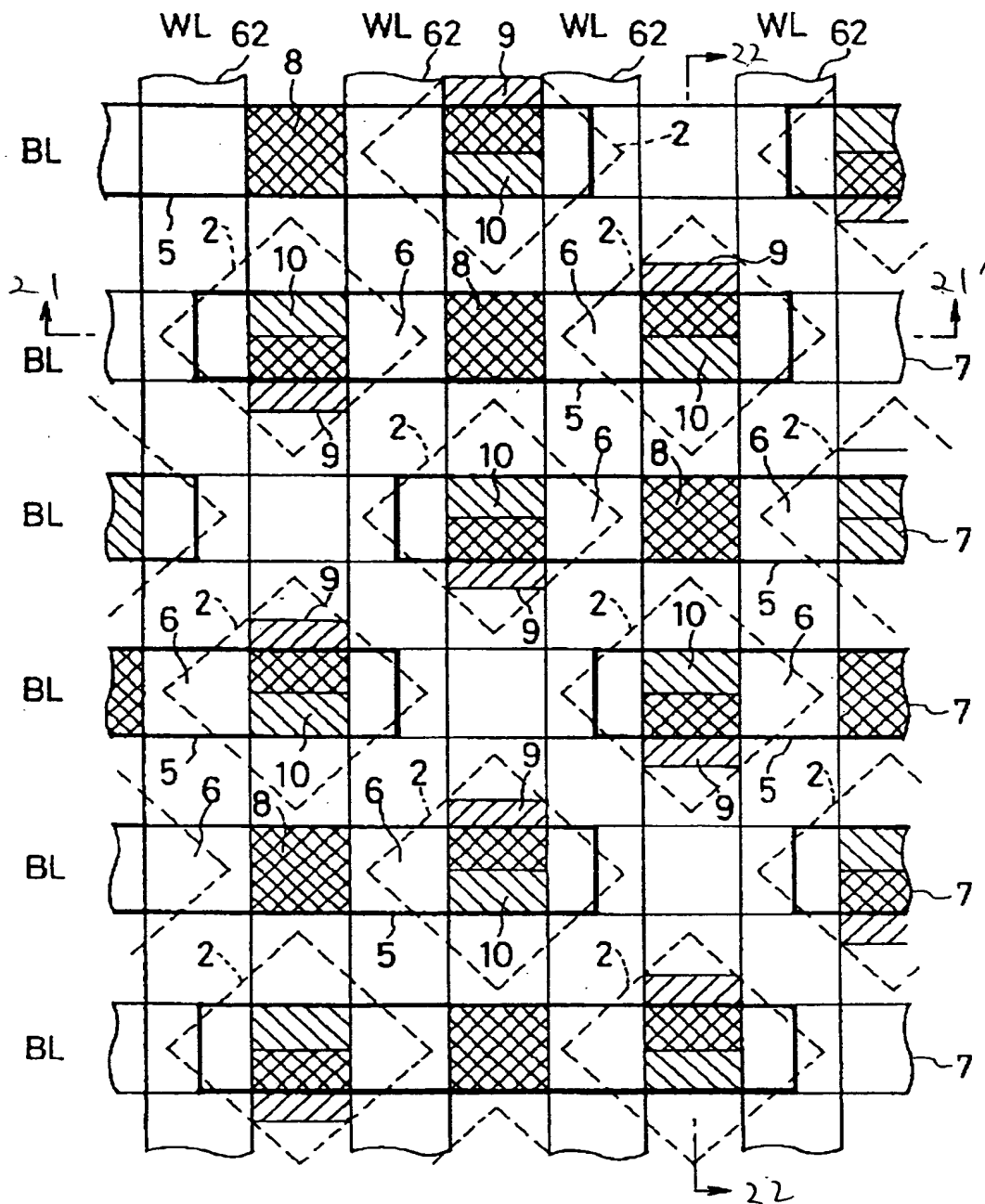


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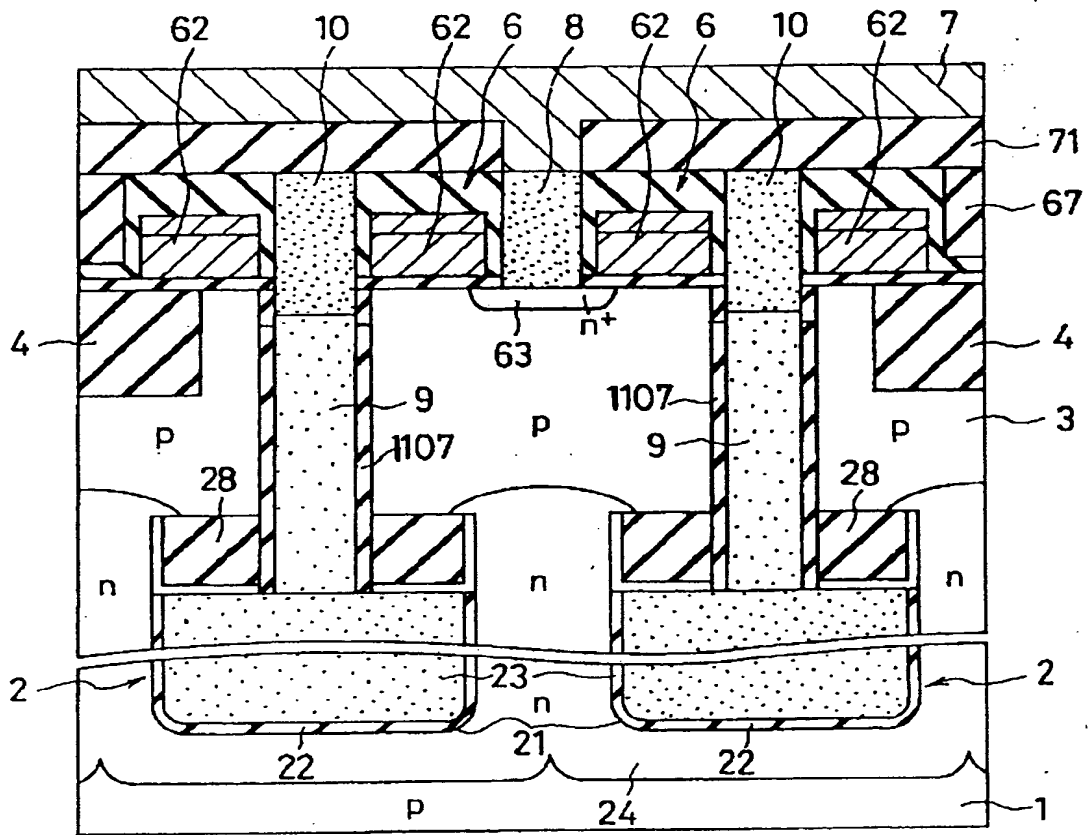


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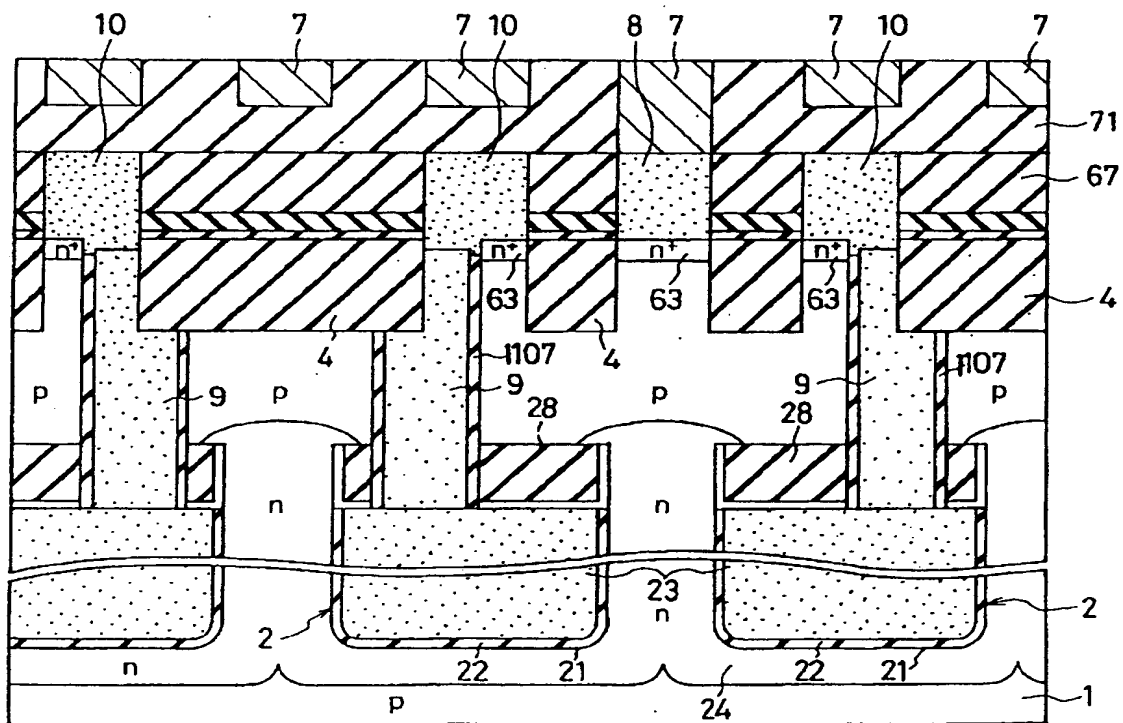


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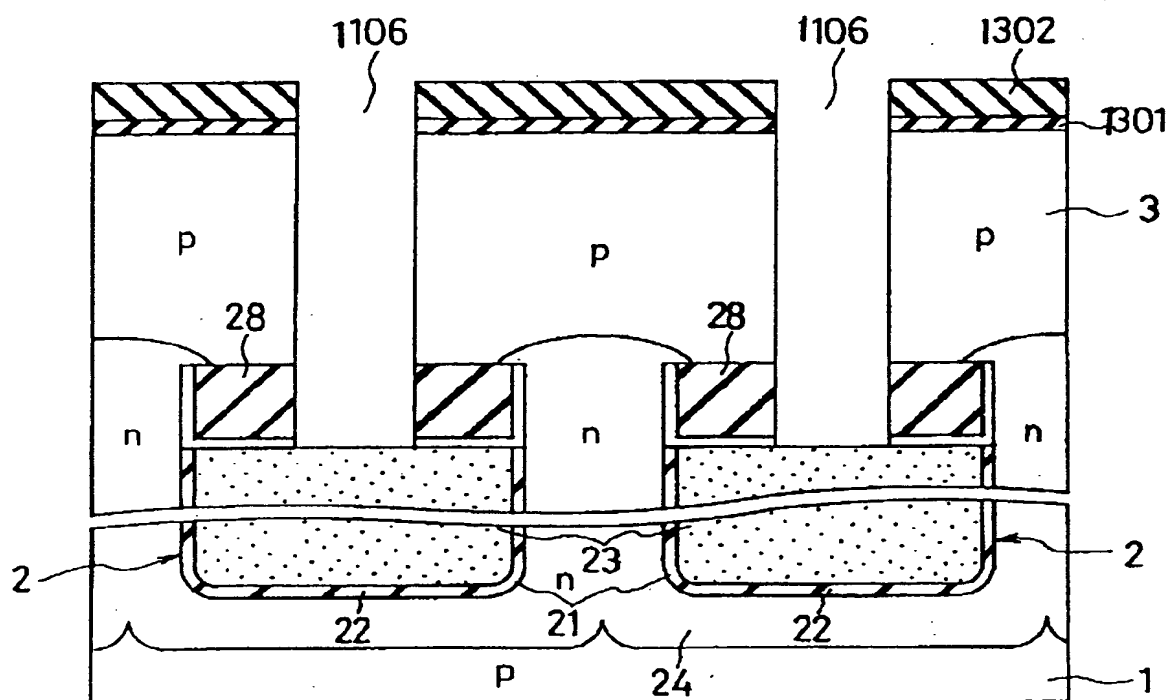


Figure 23A

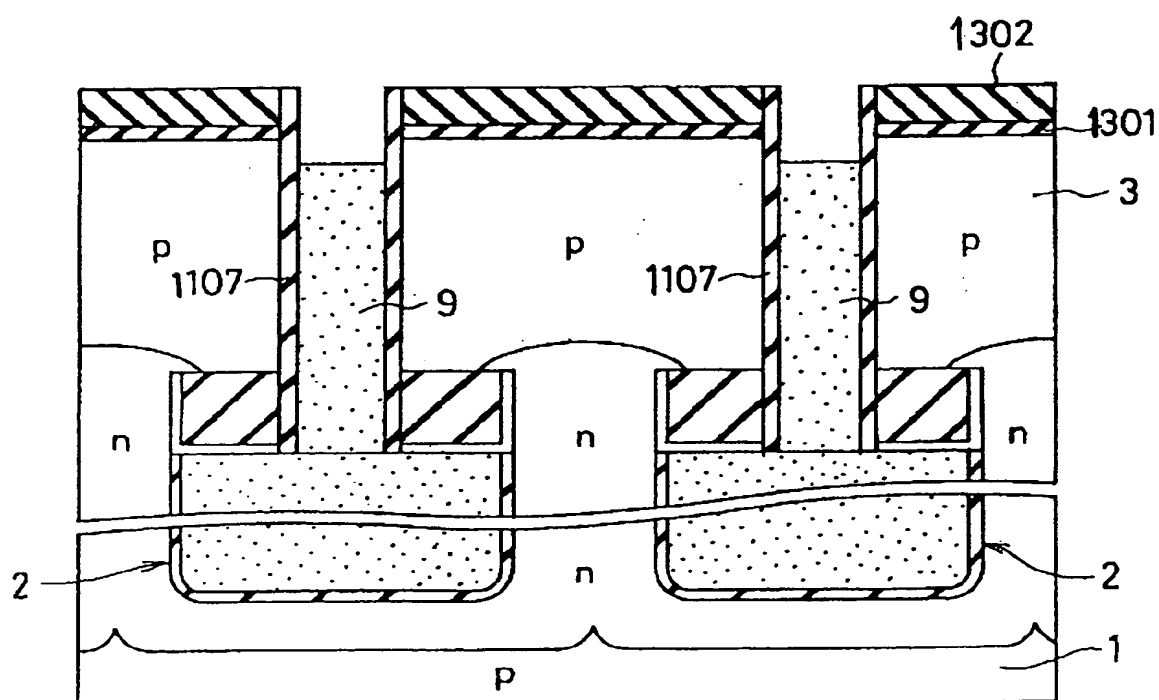


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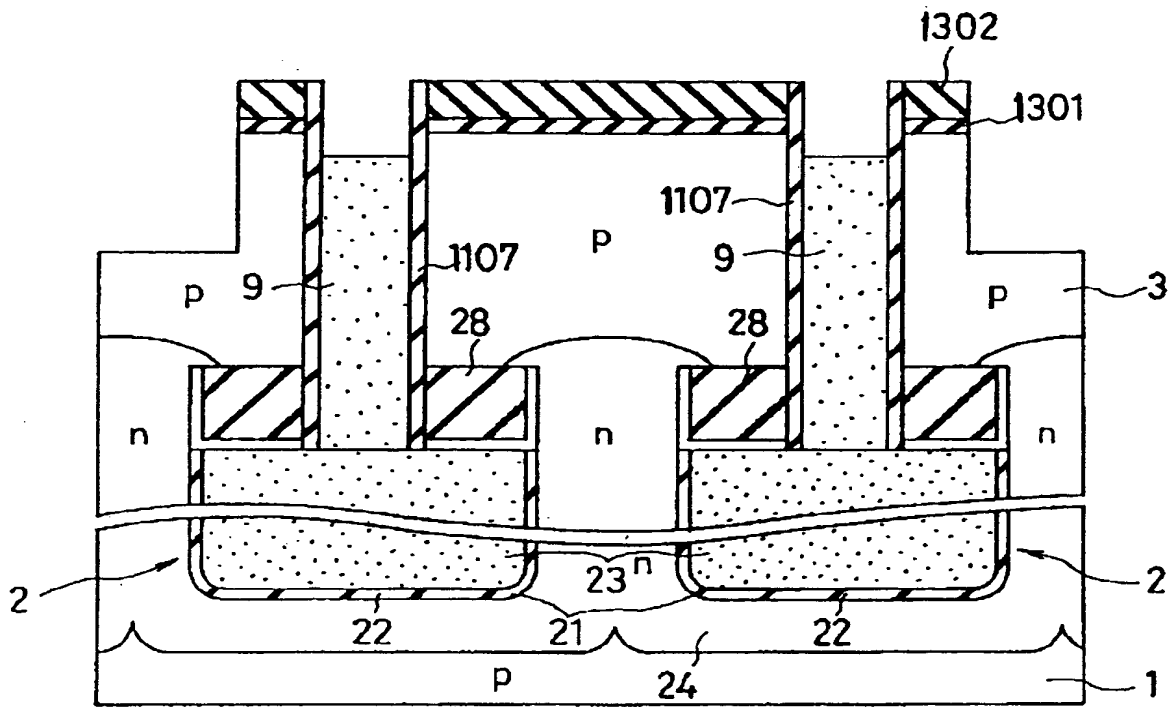


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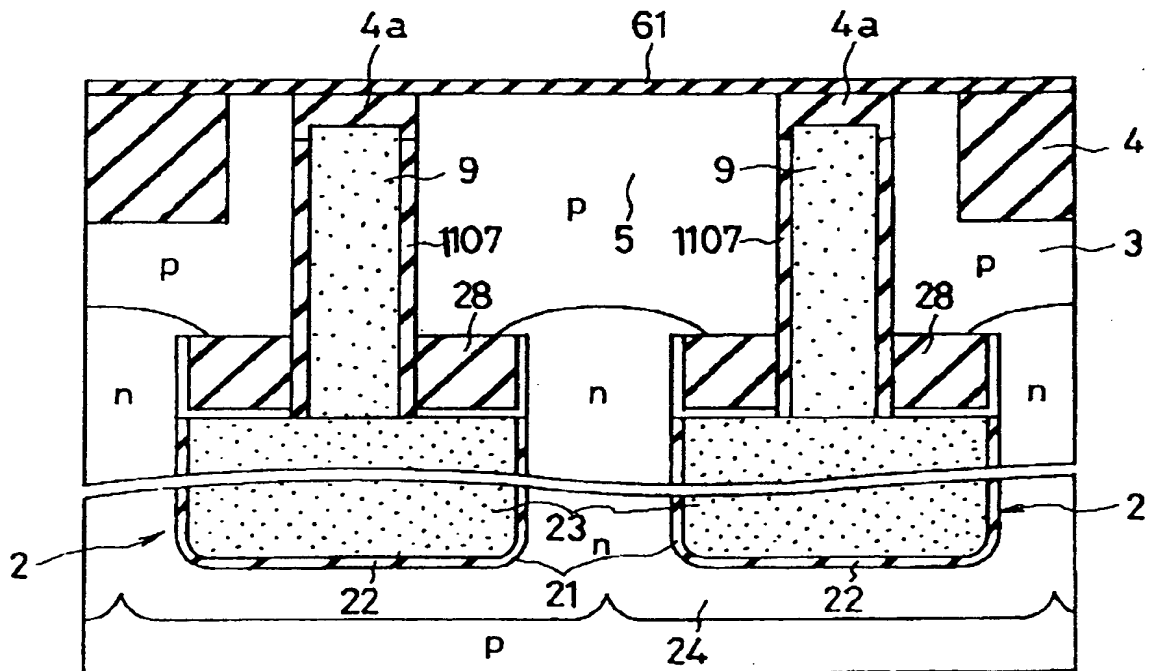


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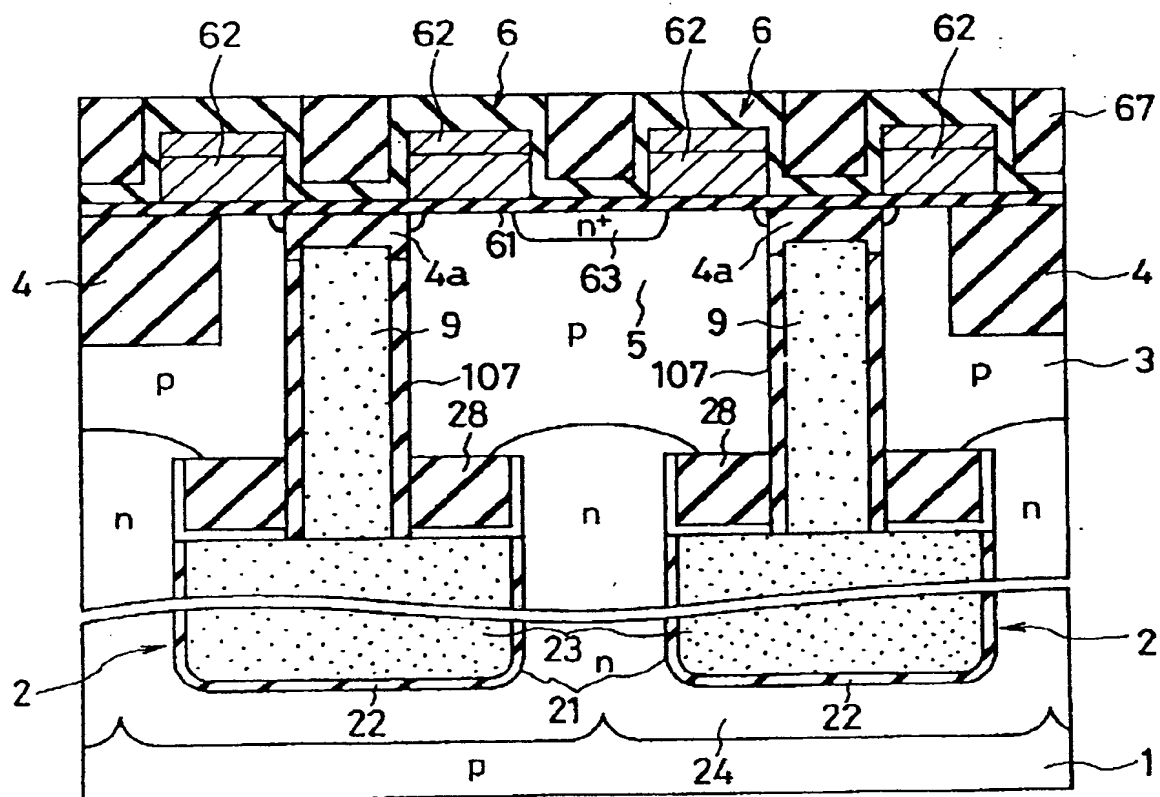


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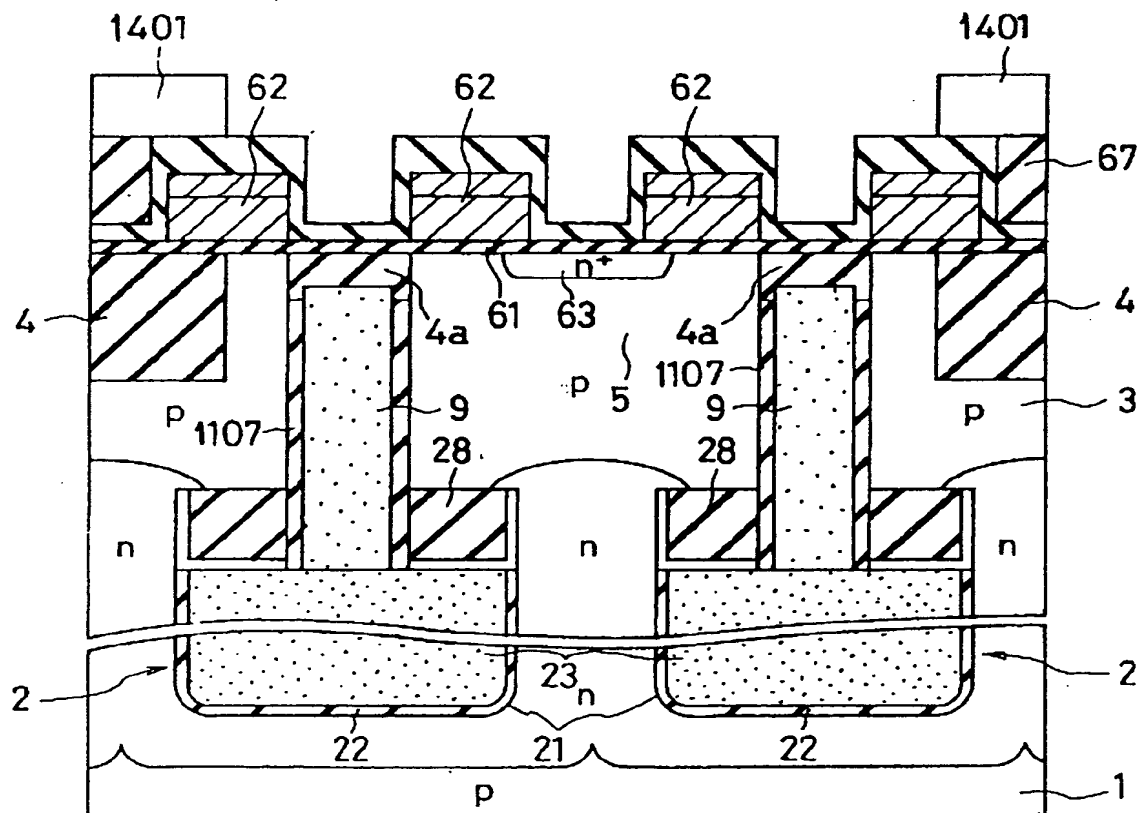


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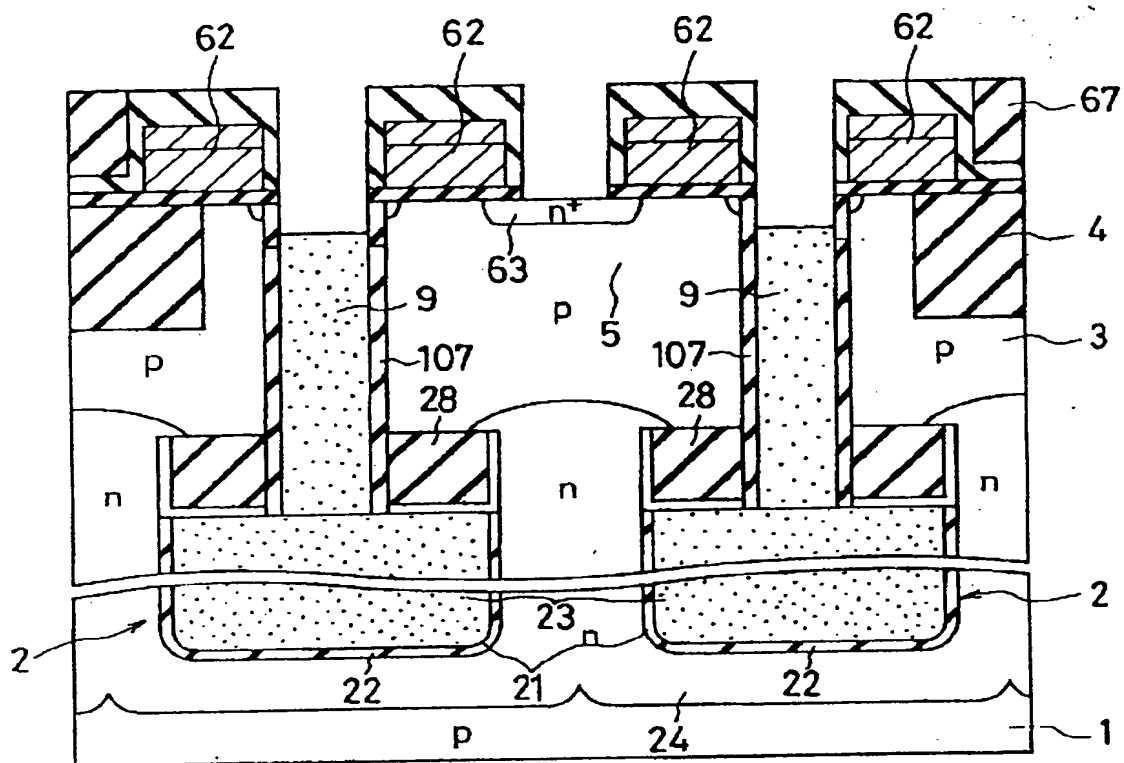


Figure 23G

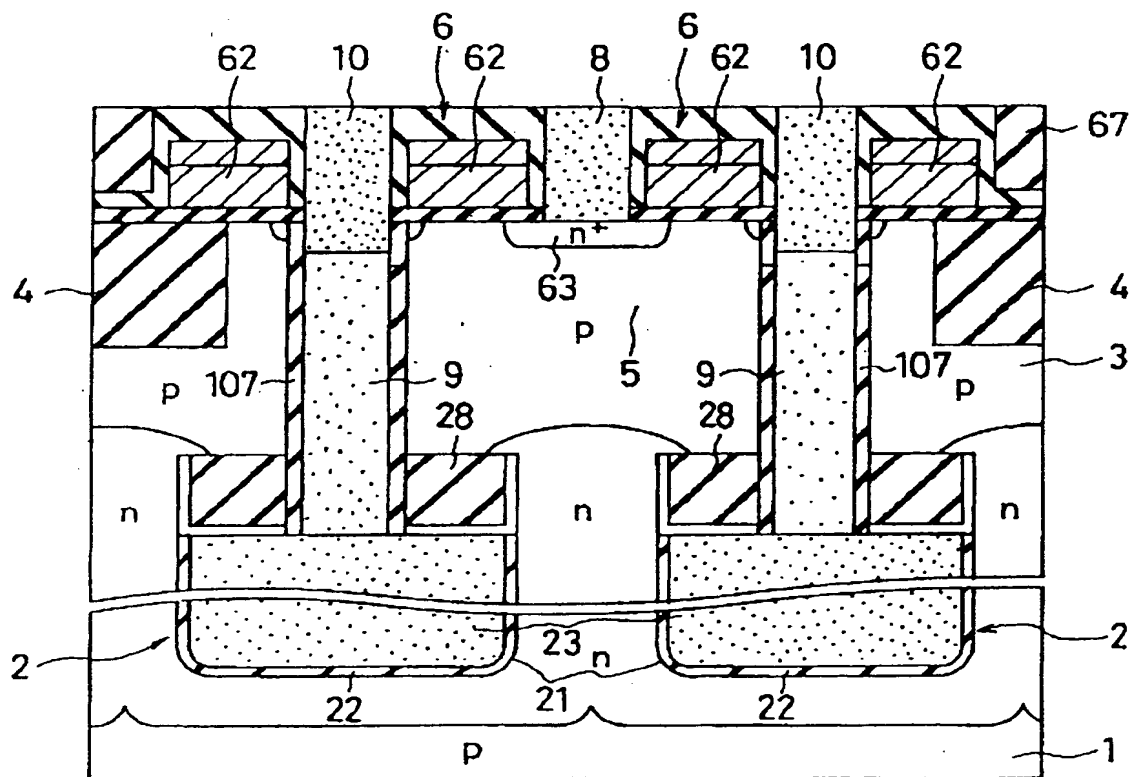


Figure 23H

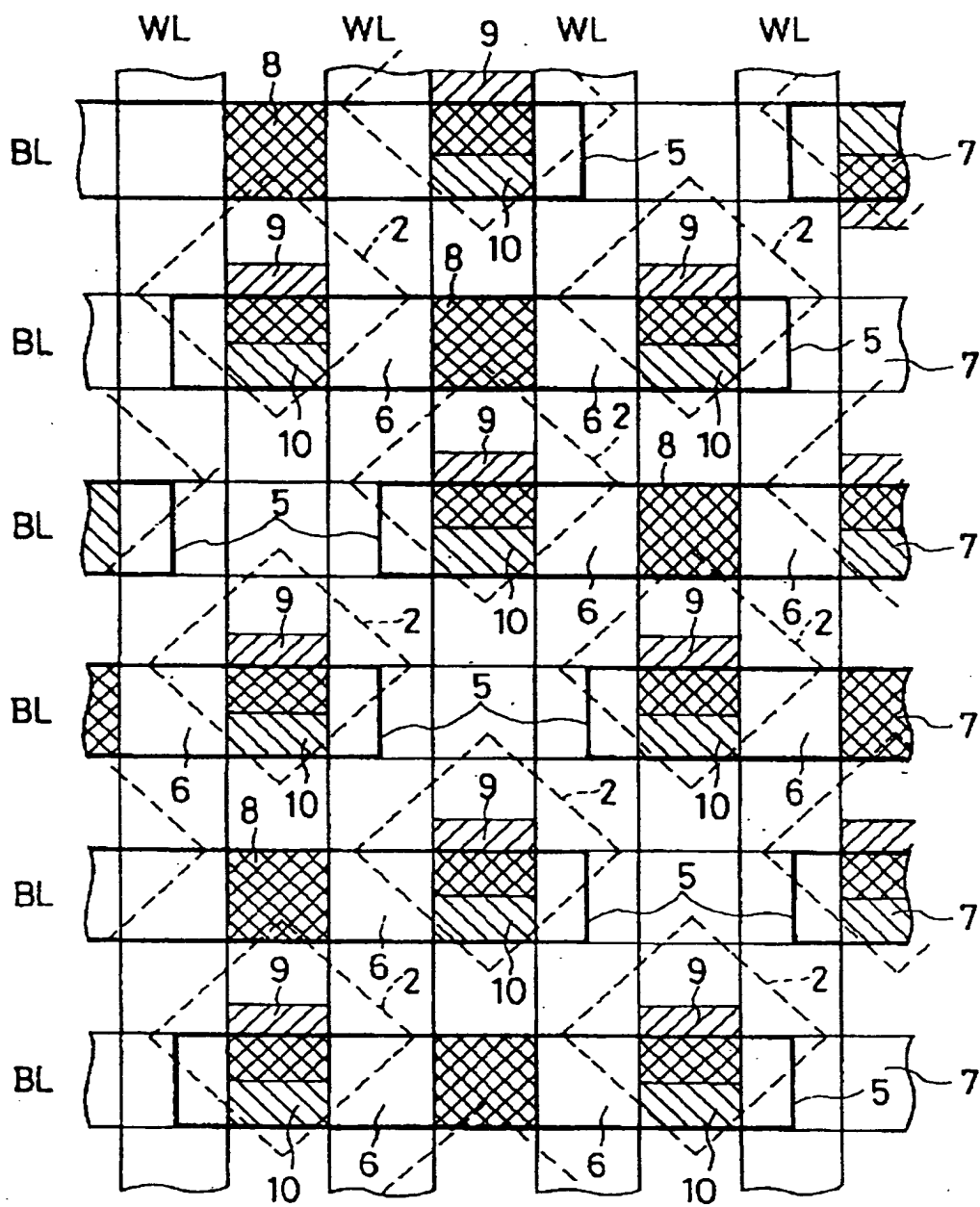


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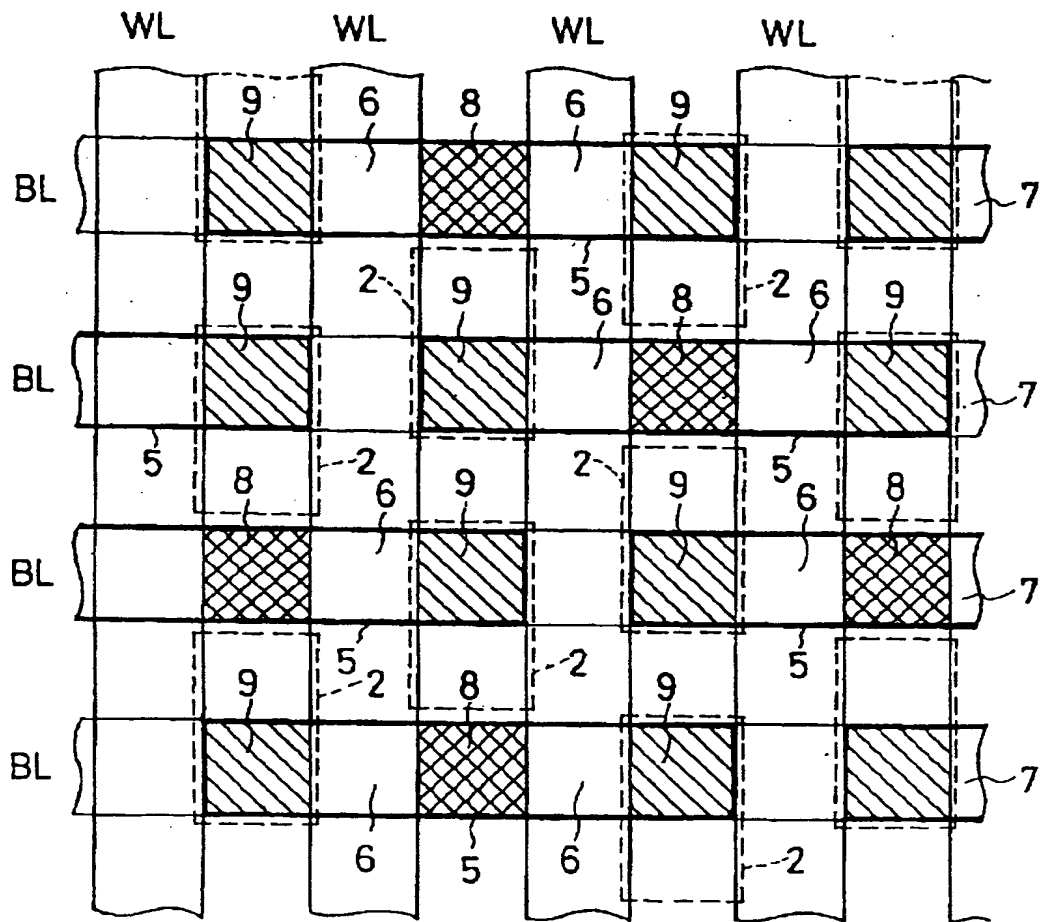


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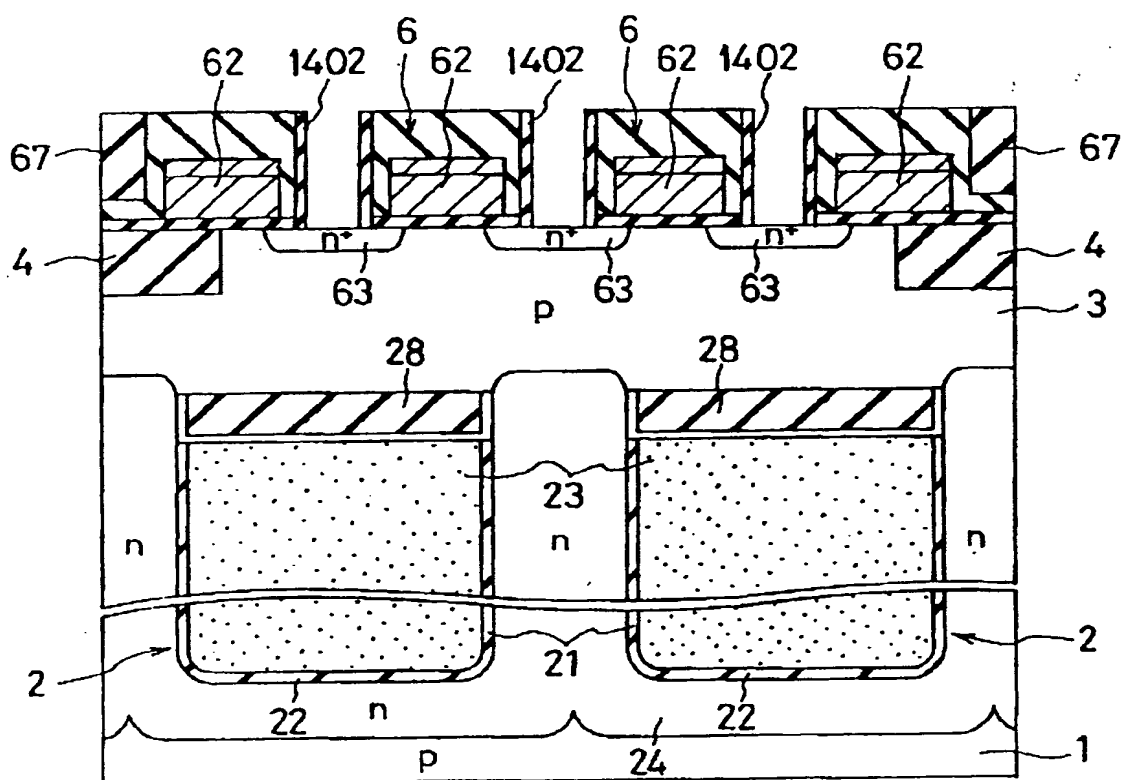


Figure 26A

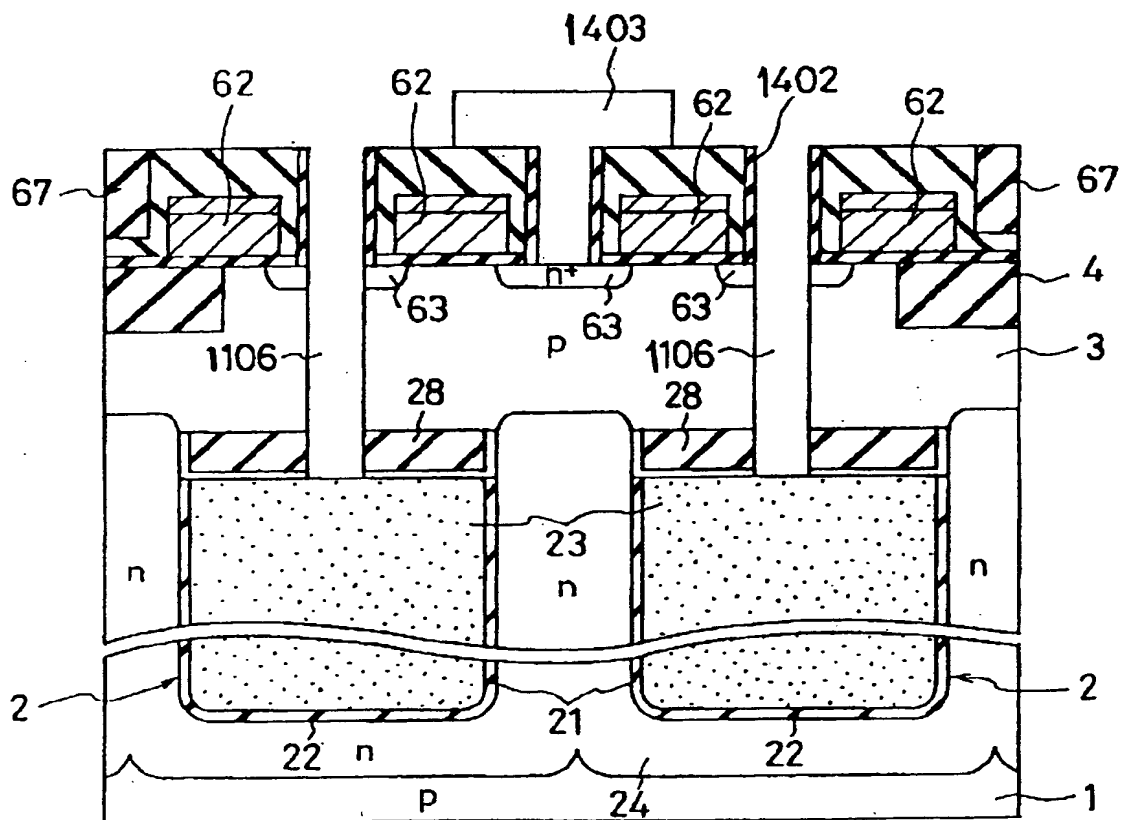
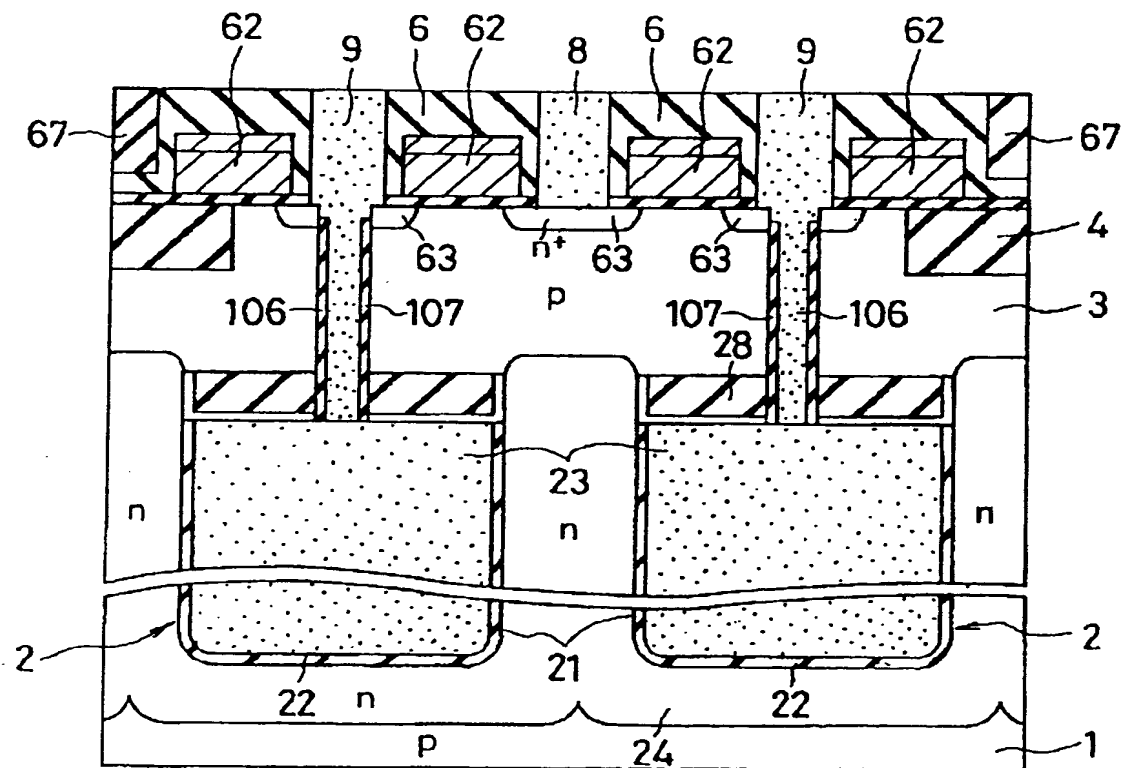
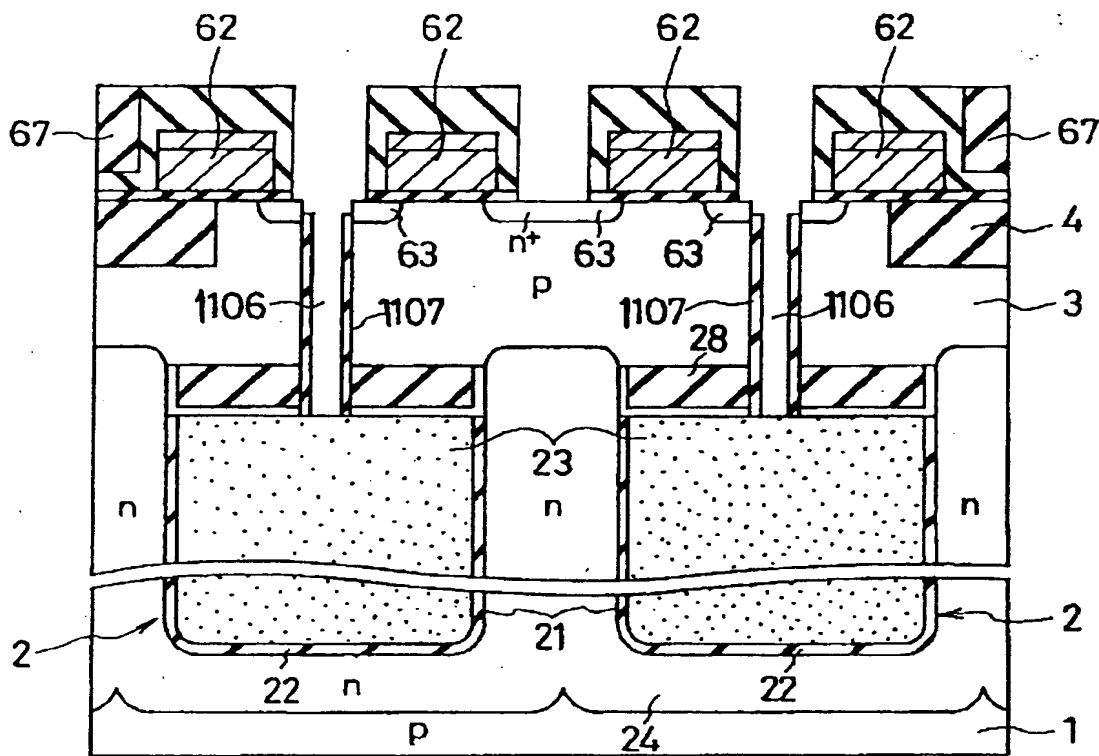


Figure 26B



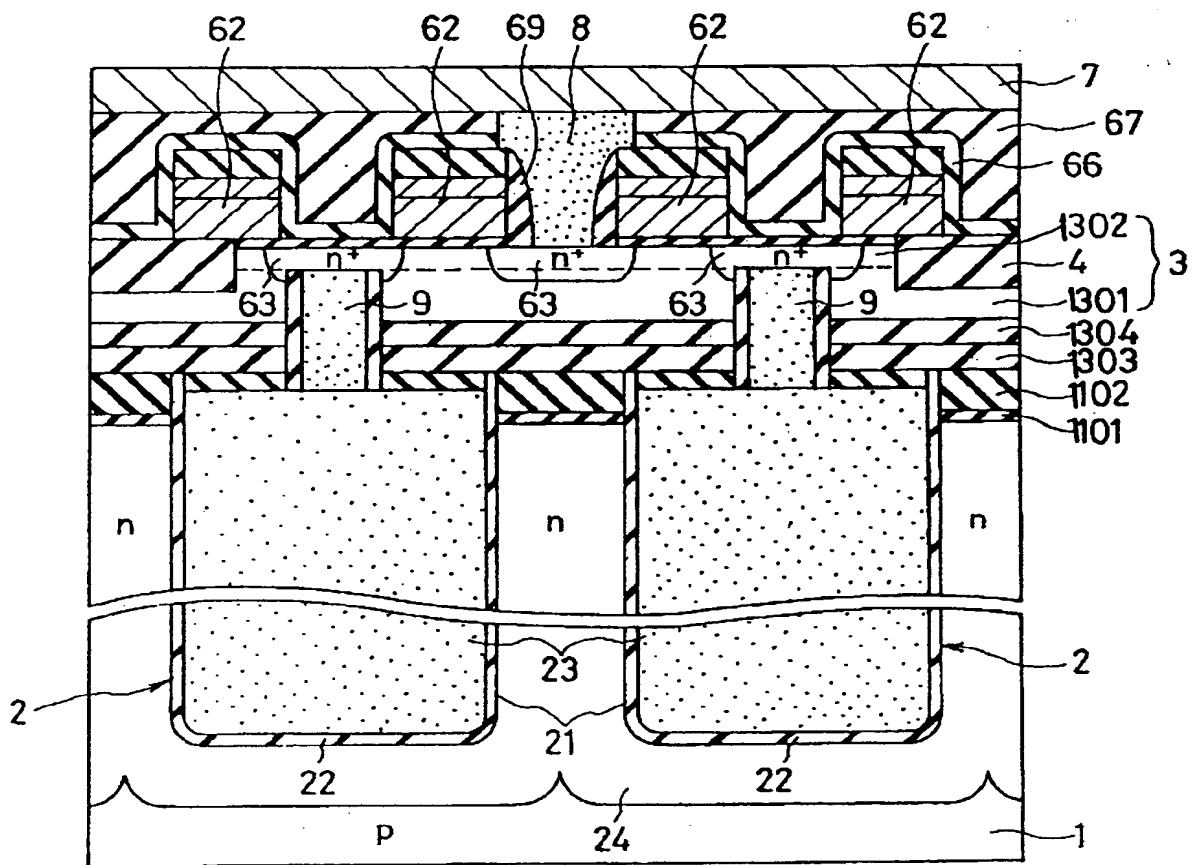


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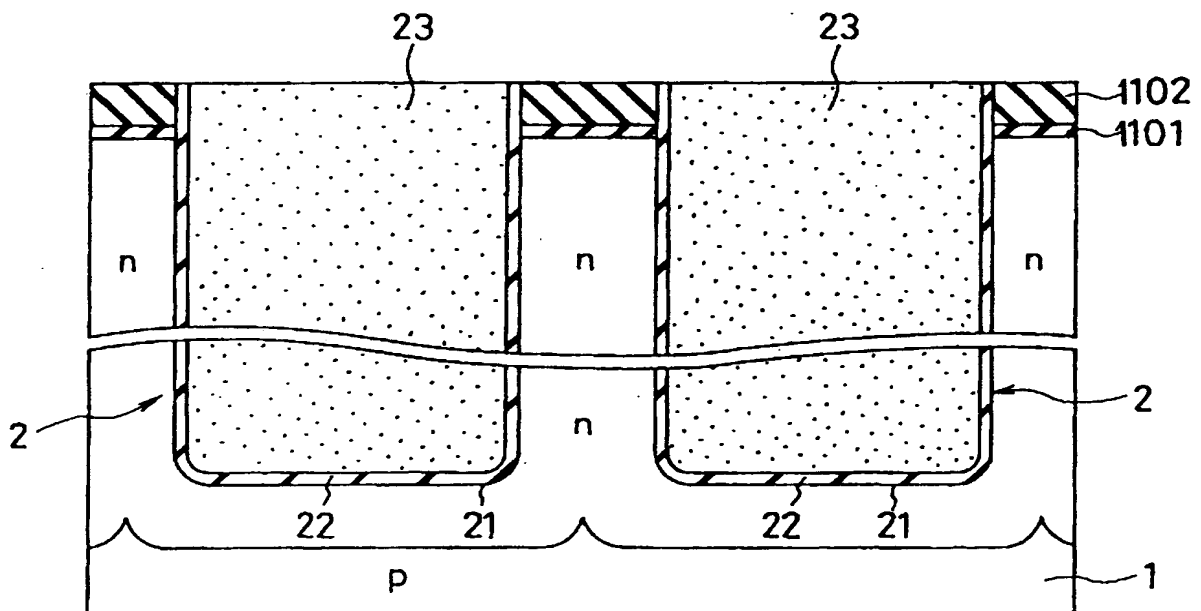


Figure 28A



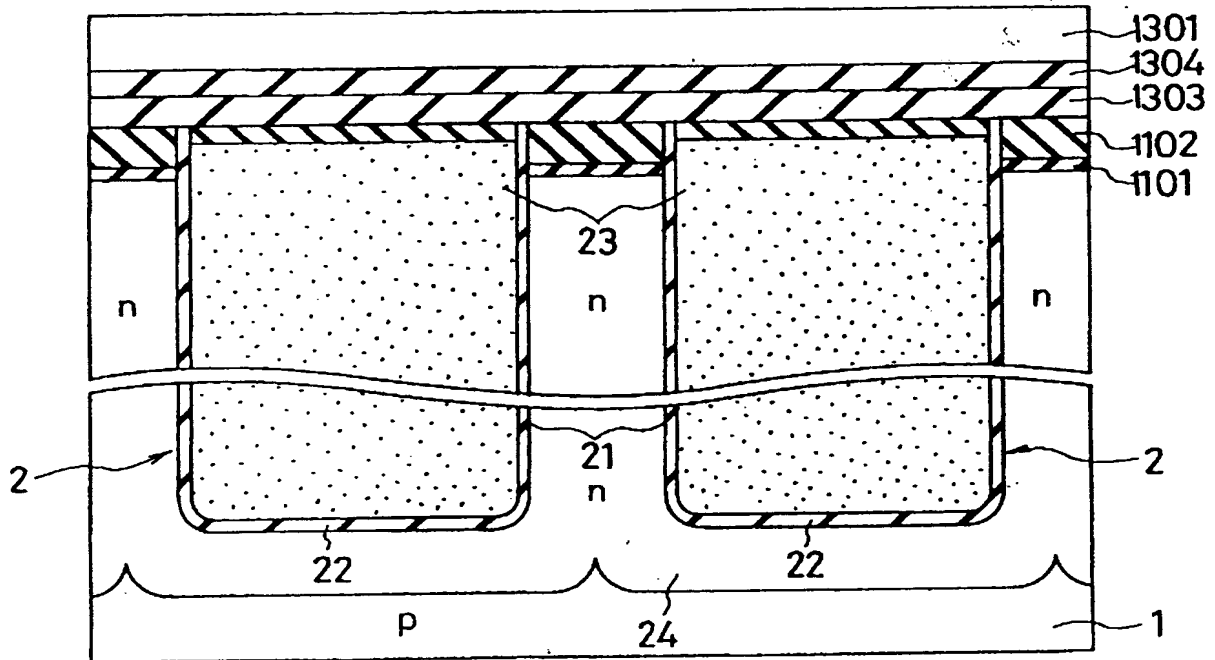


Figure 28B

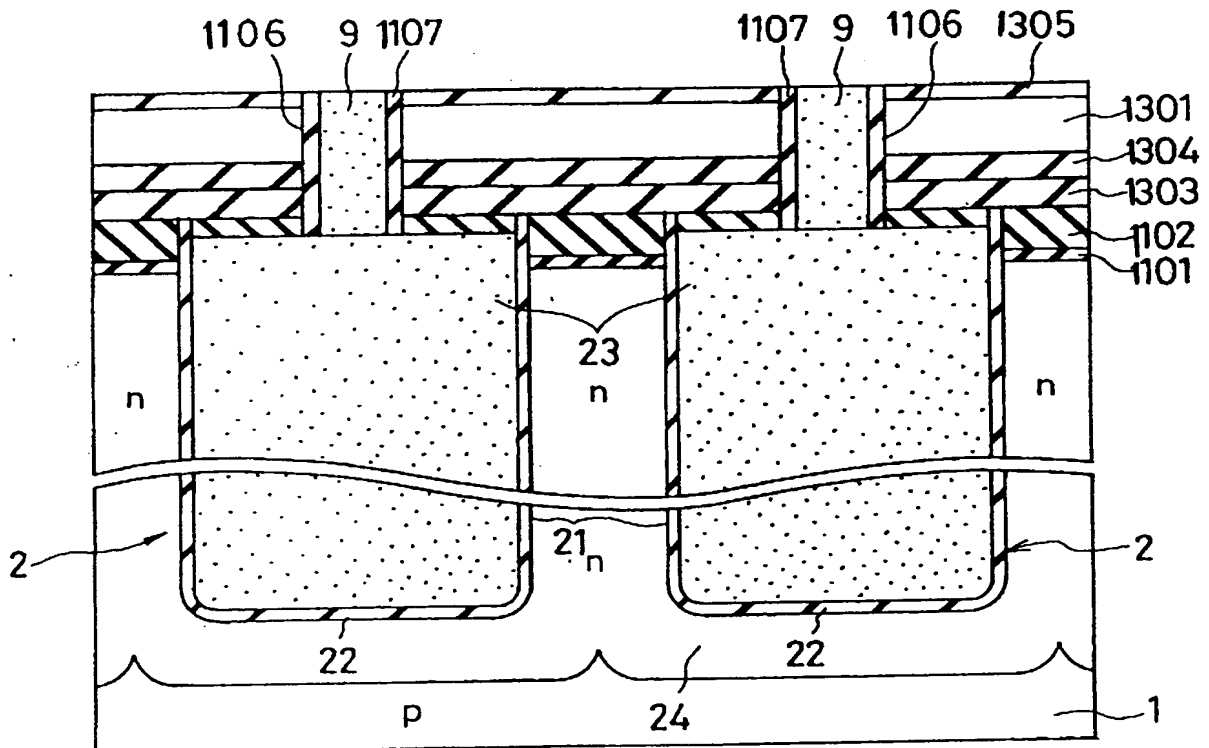


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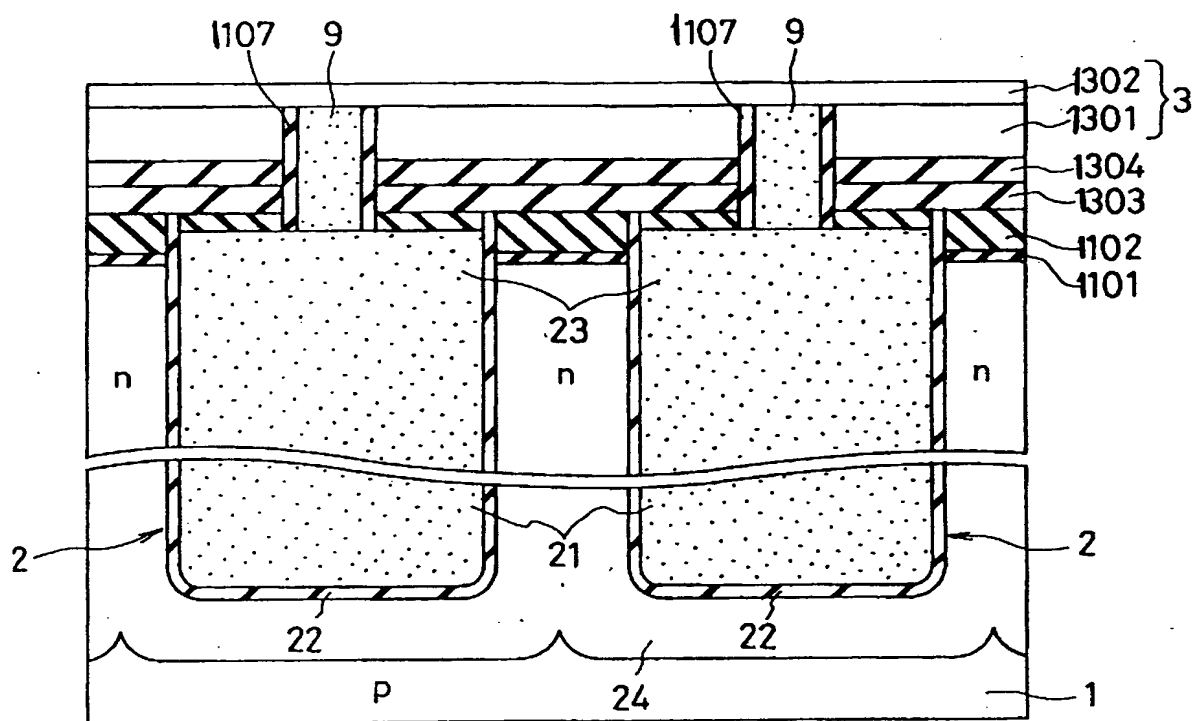


Figure 28-D

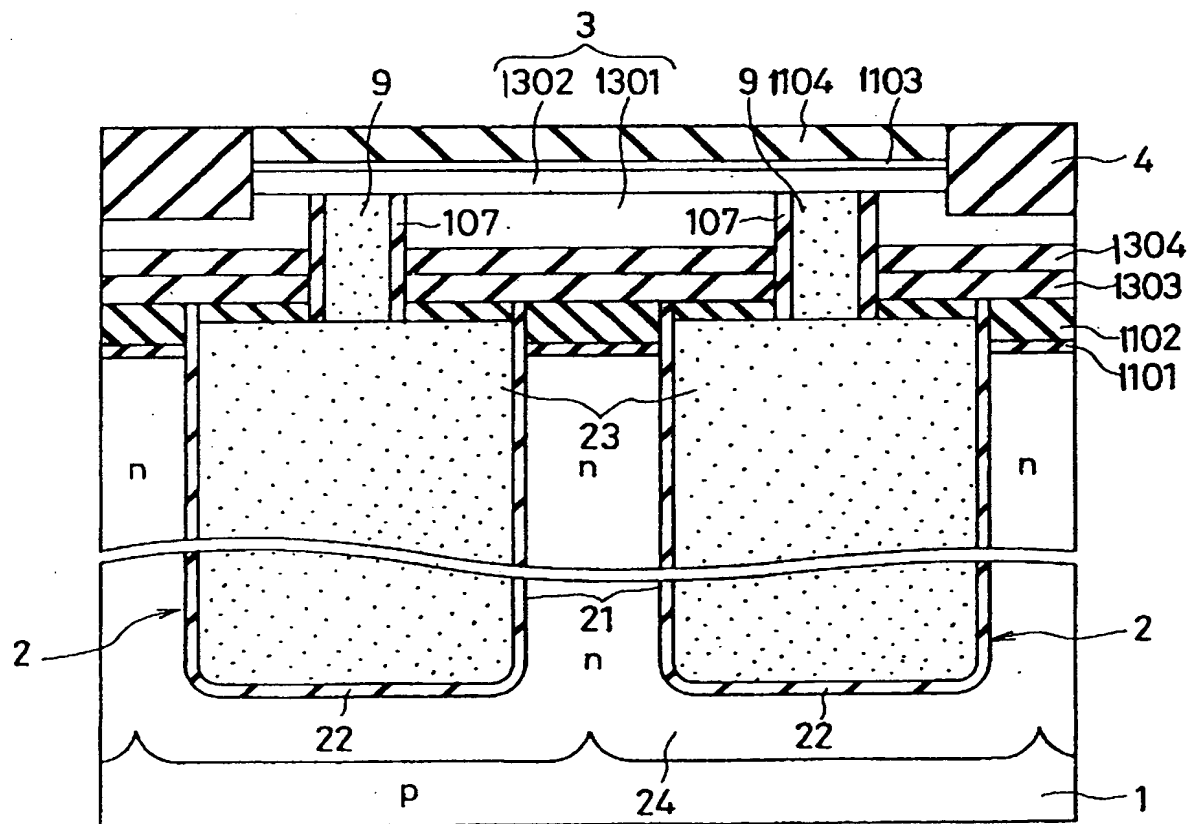


Figure 28E



Figure 28F

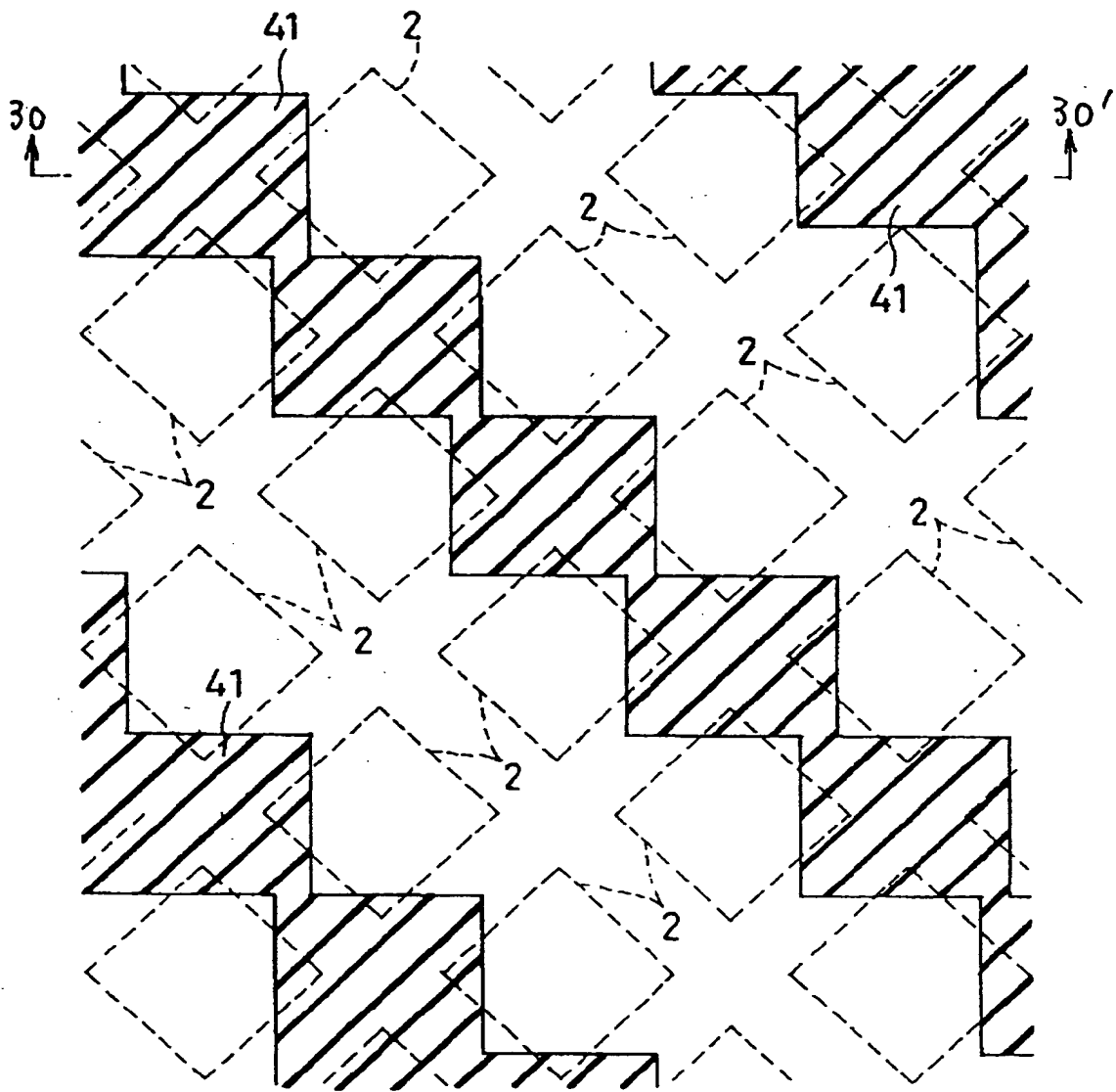


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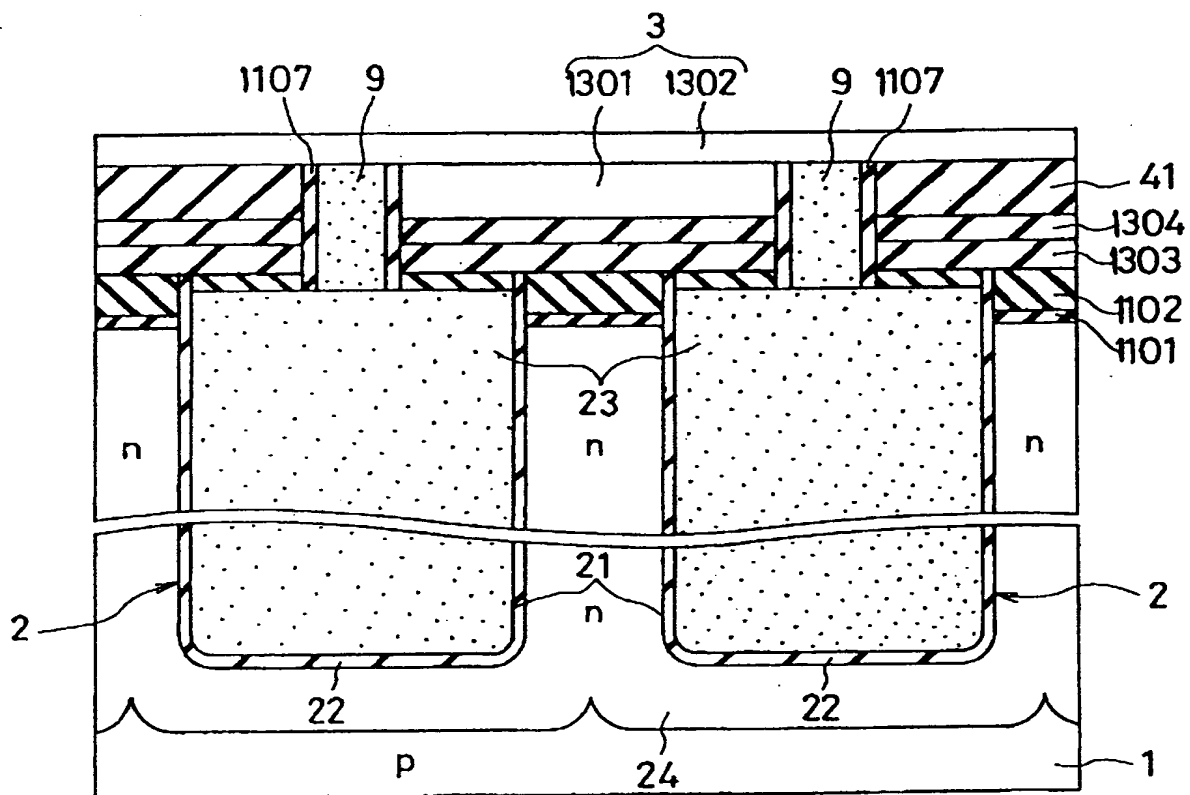


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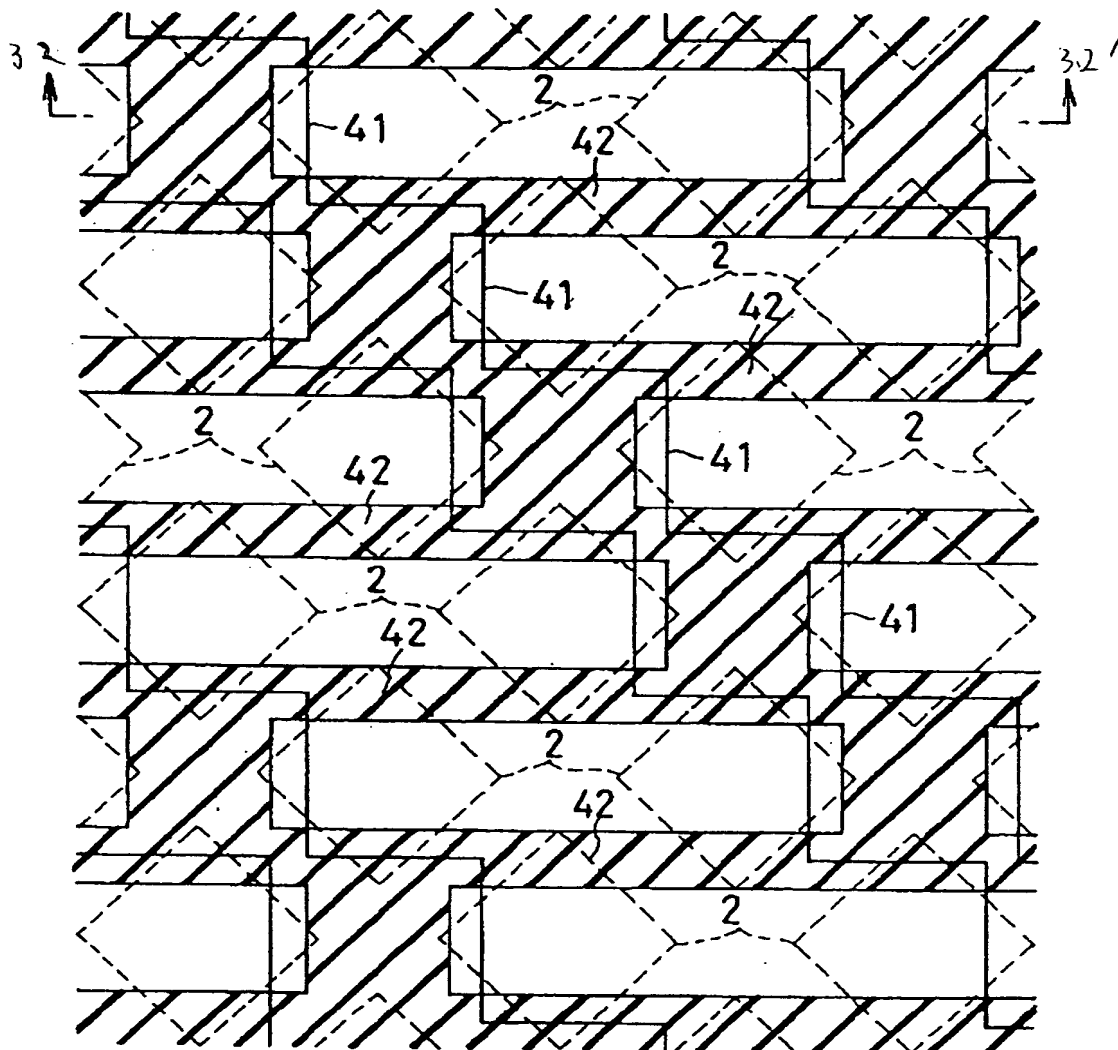


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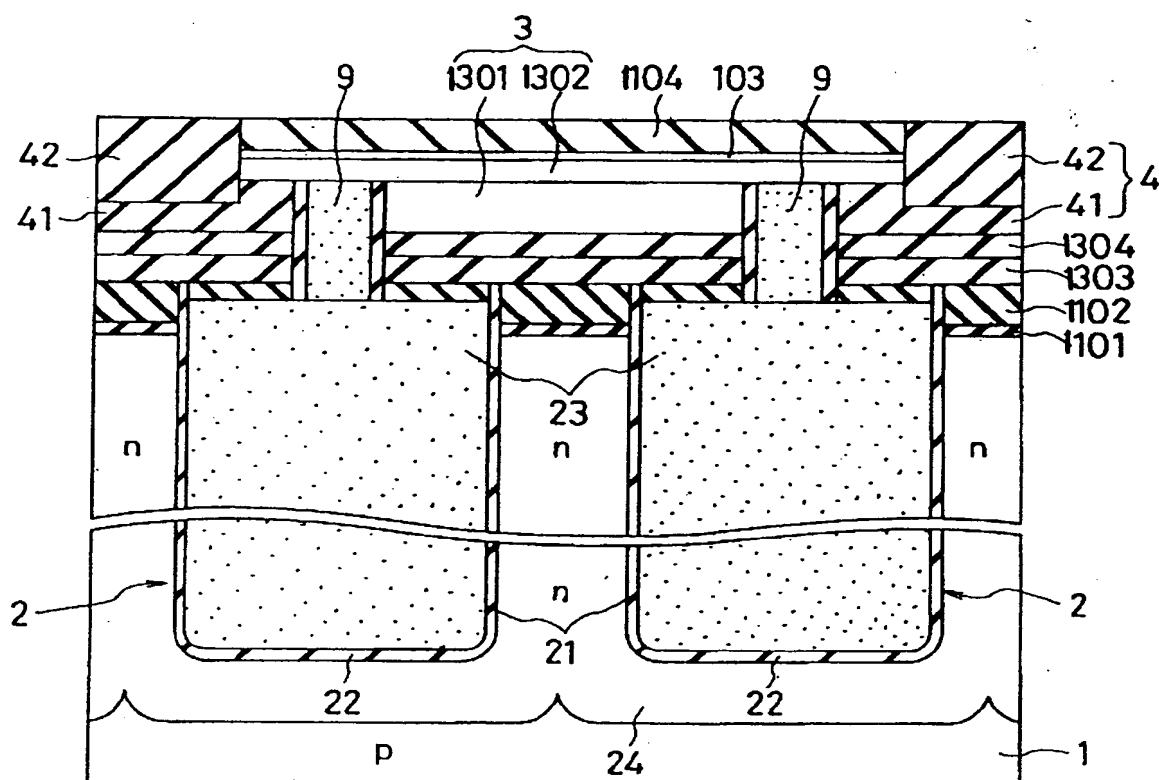


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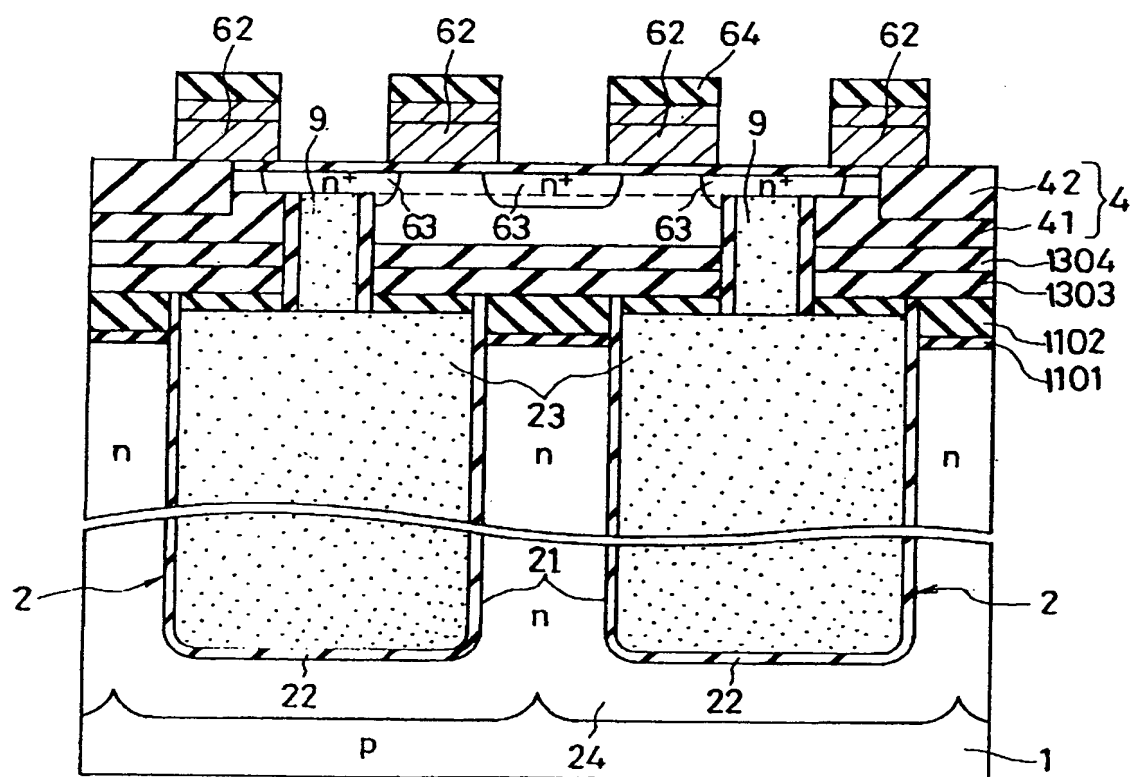


Figure 33